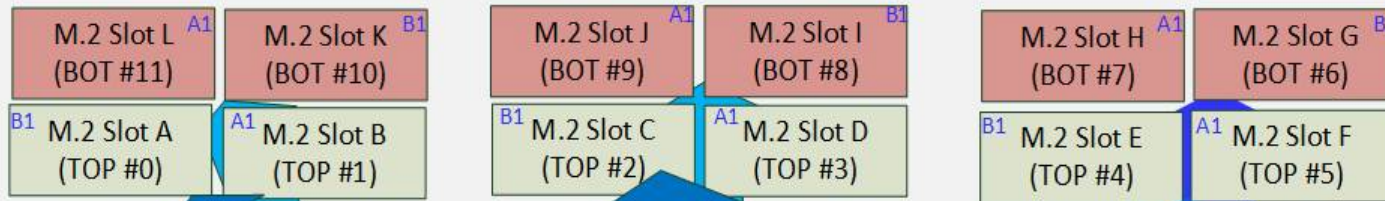


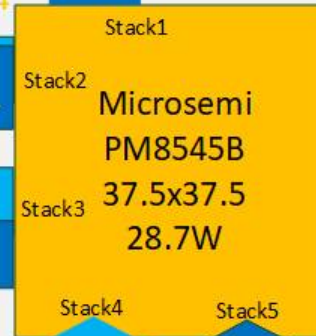
GLACIER POINT V2
Carrier Board

INDEX

1	Cover Page	41	INA230 / I2C MUX 7
2	Page Index	42	I2C MUX 1-3
3	Block Diagram	43	I2C MUX 4-6
4	PCIe Topology	44	P3V3 M.2 POWER Switch 1
5	Block Diagram - SMBus	45	P3V3 M.2 POWER Switch 2
6	Power Sequence	46	P3V3 M.2 POWER Switch 3
7	Power Distribution	47	P3V3 M.2 POWER Switch 4
8	Block Diagram - Clock	48	LED
9	Block Diagram - Reset	49	I2C GPIO
10	Block Diagram - UART&JTAG	50	Level Shifter 3
11	BLANK	51	Temperature Sensors/FRU
12	MEZZ CONN PRIMARY	52	BIC_SNOWLAKE 1
13	MEZZ CONN EXTENSION	53	BIC_SNOWLAKE 2
14	PCIE SWITCH (STACK1-2)	54	BIC_SNOWLAKE 3
15	PCIE SWITCH (STACK3-4)	55	Level Shifter 4
16	PCIE SWITCH (STACK5)	56	BIC-VOLTAGE MONITOR
17	PCIE SWITCH (CLOCKS/RESET)	57	CPLD 1
18	PCIE SWITCH (GPIO)	58	CPLD 2
19	PCIE SWITCH (PWR1/VSS1)	59	CPLD 3
20	PCIE SWITCH (PWR2/VSS2)	60	MISC 1
21	PCIE SWITCH (PWR3/VSS3)	61	MISC 2
22	SPI FLASH/EEPROM/JTAG	62	P3V3 STBY
23	PCIE SWITCH UART	63	P0V92
24	100MHz CLOCK GEN	64	P1V8
25	CLOCK BUFFER 1	65	Mechanical/Delta-L
26	CLOCK BUFFER 2	66	TDR
27	LEVEL SHIFTER 1	67	DUMMY SYMBOL
28	LEVEL SHIFTER 2		
29	M.2 A		
30	M.2 B		
31	M.2 C		
32	M.2 D		
33	M.2 E		
34	M.2 F		
35	M.2 G		
36	M.2 H		
37	M.2 I		
38	M.2 J		
39	M.2 K		
40	M.2 L		



Glacier Point V2



Gen3 x8

Gen3 x16

120 pin Mezzanine(Plug)

160 pin Mezzanine(Plug)

120 pin Mezzanie(Recep)

160 pin Mezzanie(Recep)

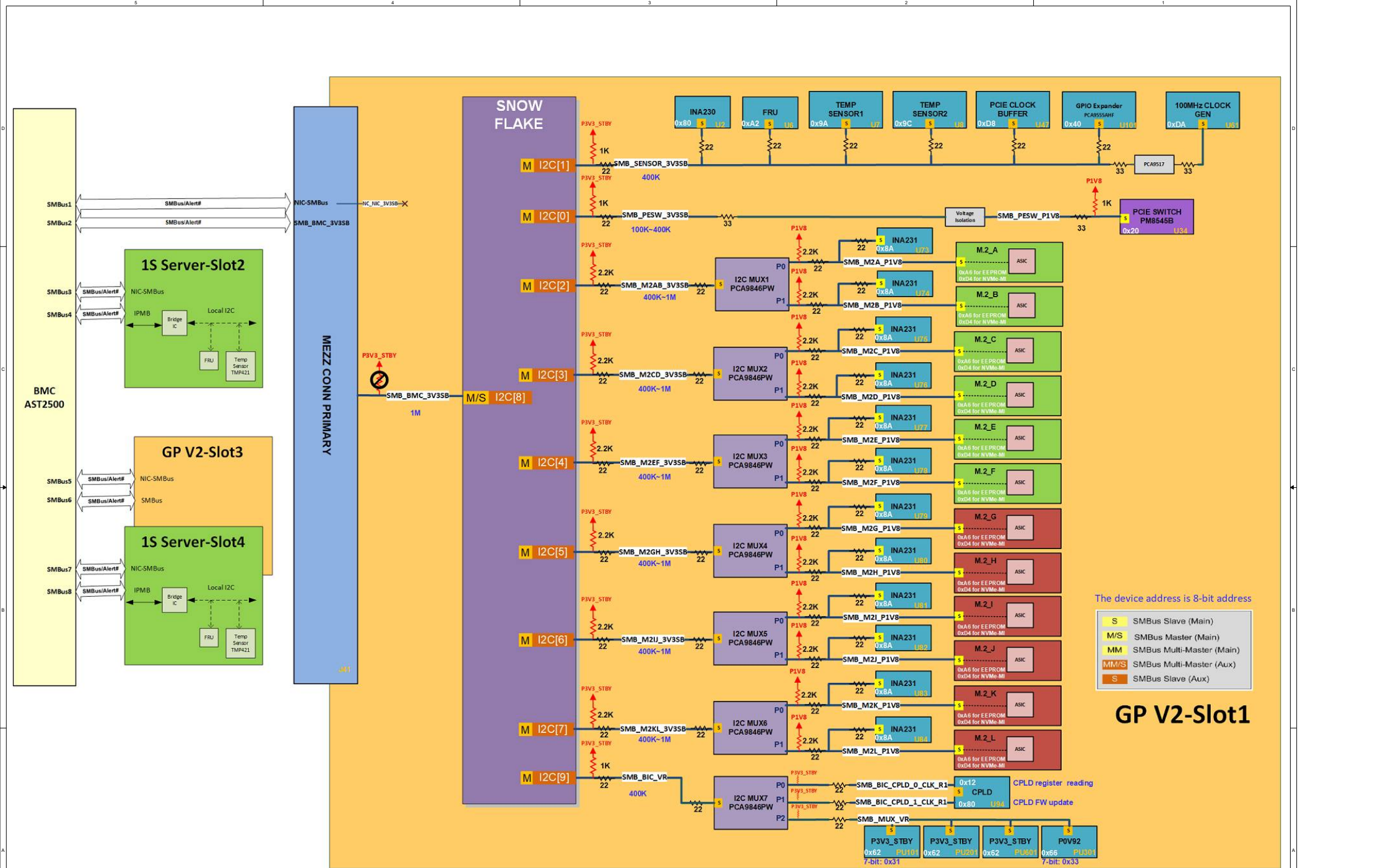
Gen3 x8

Gen3 x16

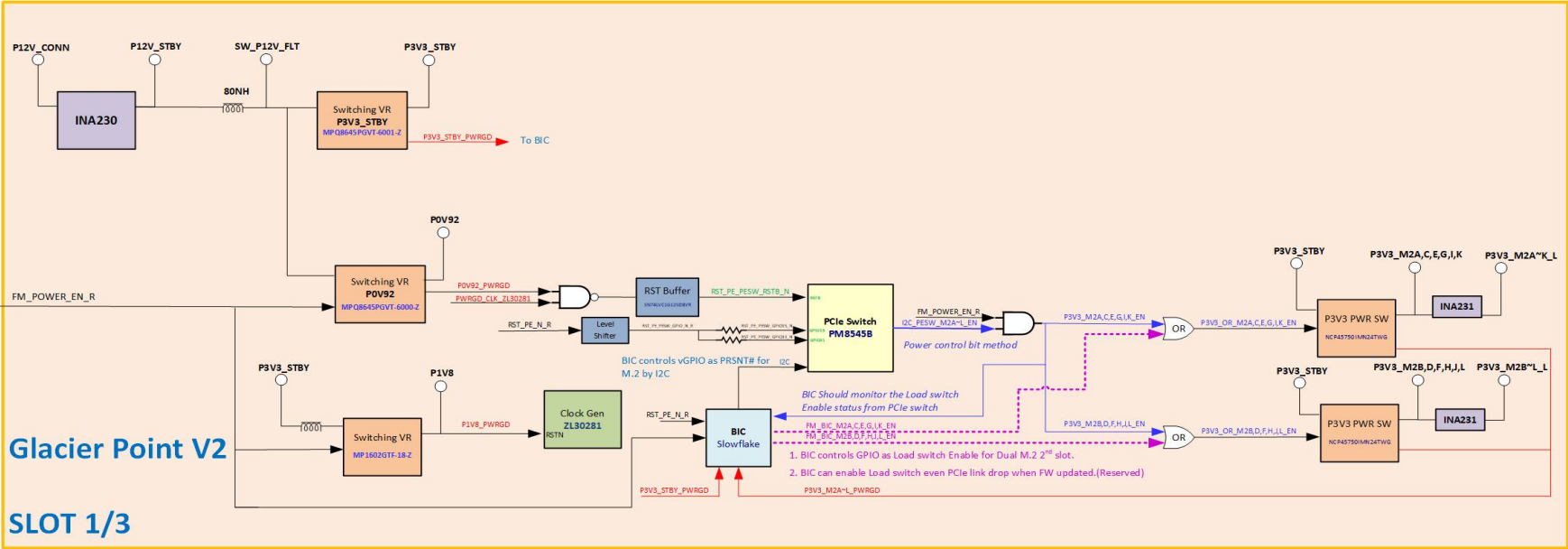
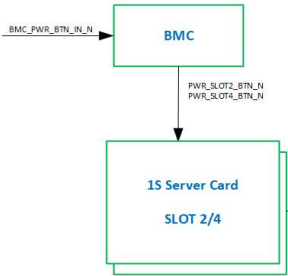
Primary

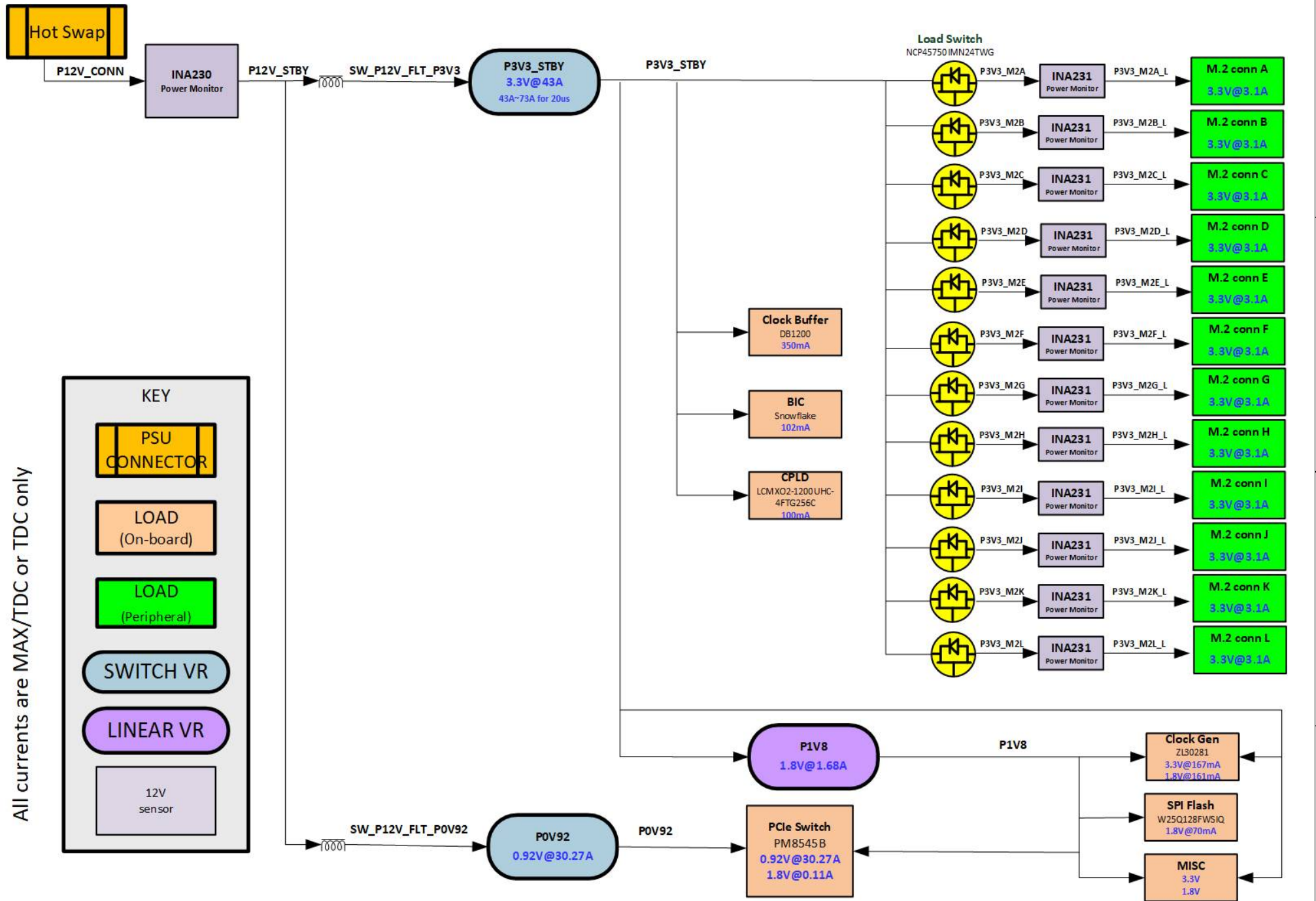
Extension

Riser Board

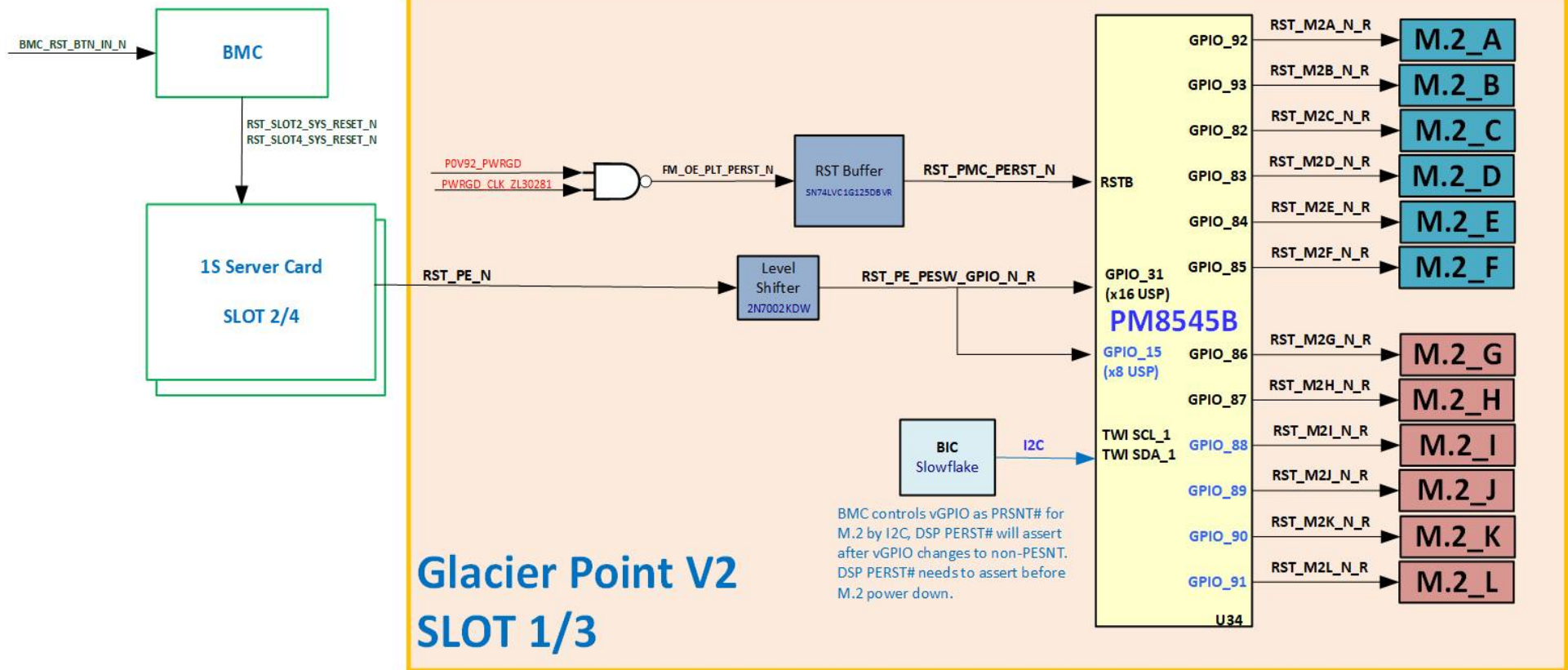


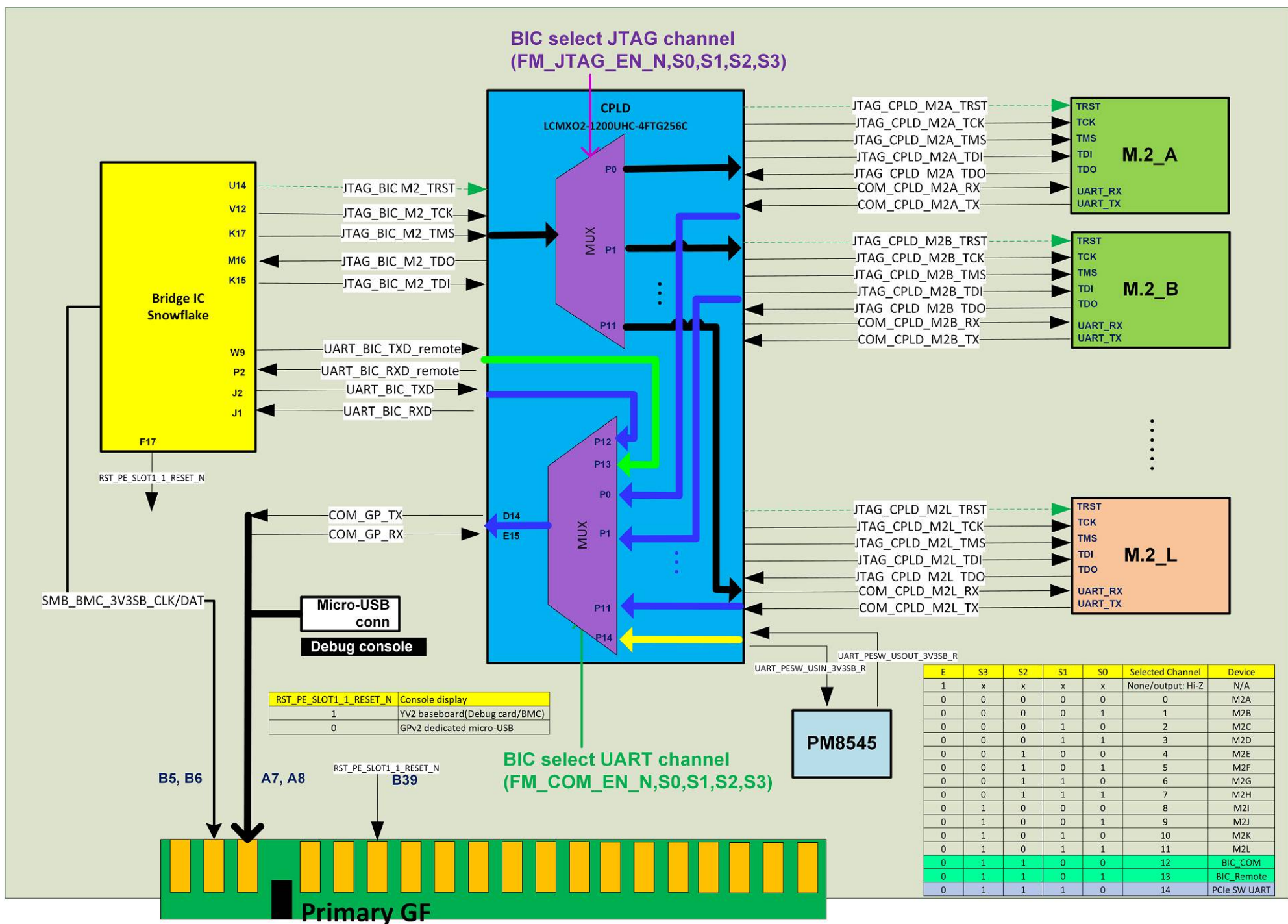
Block Diagram - SMBus





Power Distribution





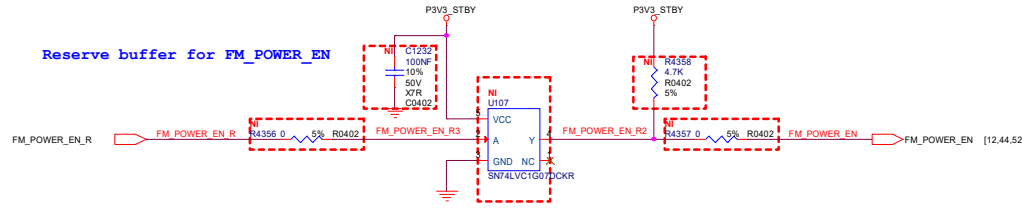
E	S3	S2	S1	S0	Selected Channel	Device
1	x	x	x	x	None/output: Hi-Z	N/A
0	0	0	0	0	0	M2A
0	0	0	0	1	1	M2B
0	0	0	1	0	2	M2C
0	0	0	1	1	3	M2D
0	0	1	0	0	4	M2E
0	0	1	0	1	5	M2F
0	0	1	1	0	6	M2G
0	0	1	1	1	7	M2H
0	1	0	0	0	8	M2I
0	1	0	0	1	9	M2J
0	1	0	1	0	10	M2K
0	1	0	1	1	11	M2L
0	1	1	0	0	12	BIC_COM
0	1	1	0	1	13	BIC_Remote
0	1	1	1	0	14	PCIe SW UART

Block Diagram - JTAG & UART

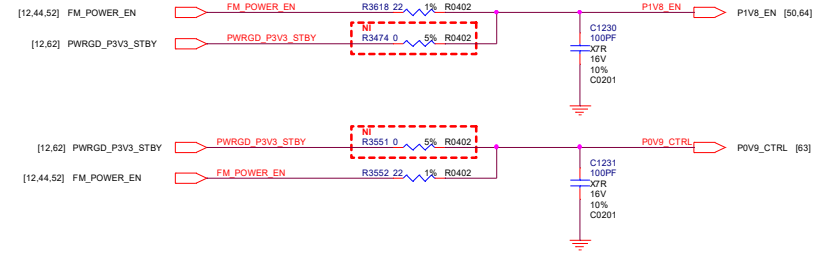


BLANK

Reserve buffer for FM_POWER_EN



SMBus and power enable connection to VR

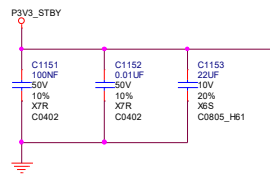


CAD Note:
C1230 place at near location(778,64 648,53)
C1231 place at near location(779,90 1327,90)

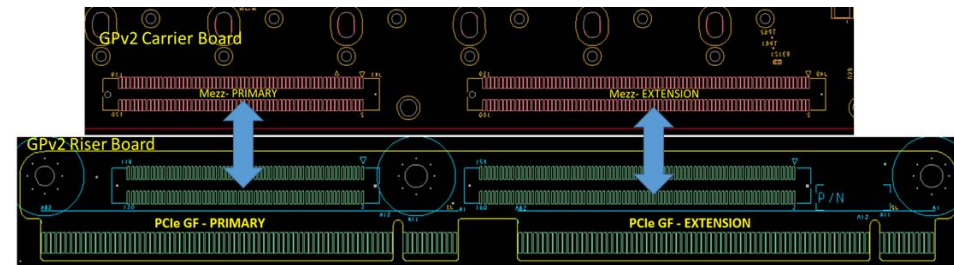
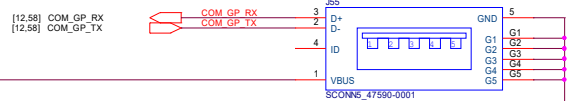
Note: Add UART signal
-- COM_GP_TX/RX

Note: Board voltage level
 $3.3V \cdot R2 / (R1 + R2) = 0.749V = GPV2$

Note: Reserved SW6
for co-layour purpose



Micro USB



Polarity Reversal for layout purpose

Polarity Reversal for layout purpose

Polarity Reversal for layout purpose

Note: Reserved USB2 (PIN25.27) port

Polarity Reversal for layout purpose

Polarity Reversal for layout purpose

Polarity Reversal for layout purpose

Polarity Reversal for layout purpose

BOM Note:
U34 change to PM8545B-FEI

Stack 1

Lane Reversal for layout purpose

Lane Reversal for layout purpose

Polarity Reversal for layout purpose

Polarity Reversal for layout purpose

Stack 2

Lane Reversal for layout purpose

Lane Reversal for layout purpose

Polarity Reversal for layout purpose

Polarity Reversal for layout purpose

BOM Note:
U34 change to PM8545B-FEI

Stack 3

Polarity Reversal for layout purpose

Polarity Reversal for layout purpose

Lane Reversal for layout purpose

Lane Reversal for layout purpose

Polarity Reversal for layout purpose

Polarity Reversal for layout purpose

Lane Reversal for layout purpose

Lane Reversal for layout purpose

Stack 4

Lane Reversal for layout purpose

Lane Reversal for layout purpose

Lane Reversal for layout purpose

Lane Reversal for layout purpose

BOM Note:
U34 change to PM8545B-FEI

Stack 5

Lane Reversal for layout purpose

Lane Reversal for layout purpose

Lane Reversal for layout purpose

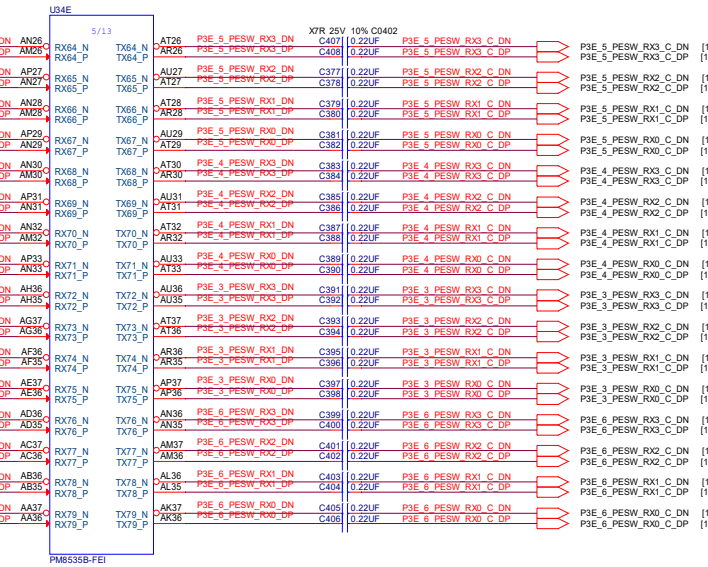
Lane Reversal for layout purpose

Lane Reversal for layout purpose

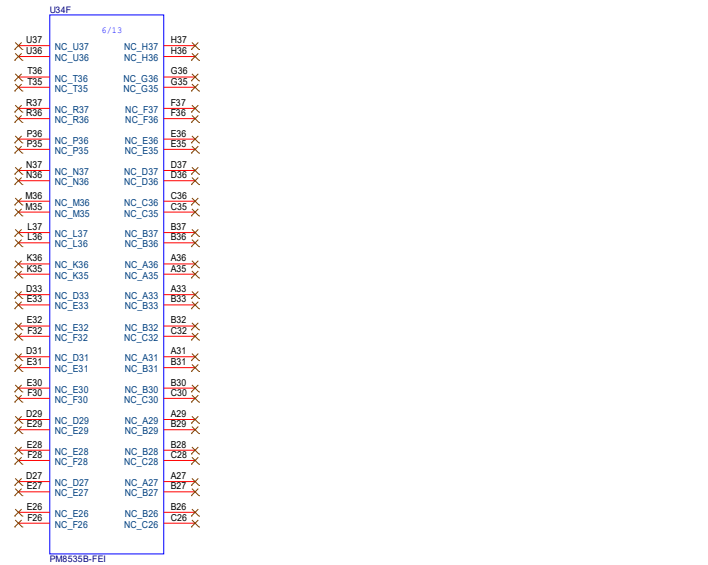
Lane Reversal for layout purpose

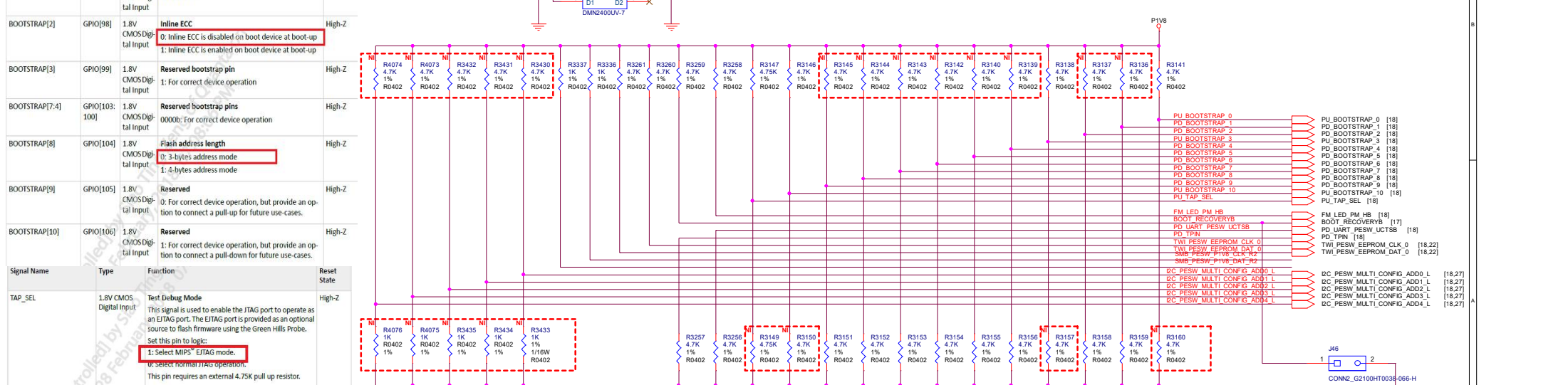
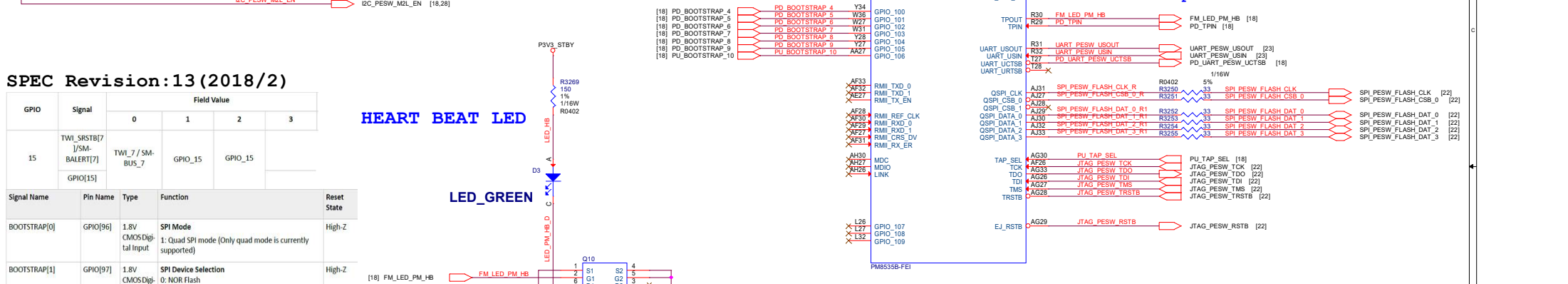
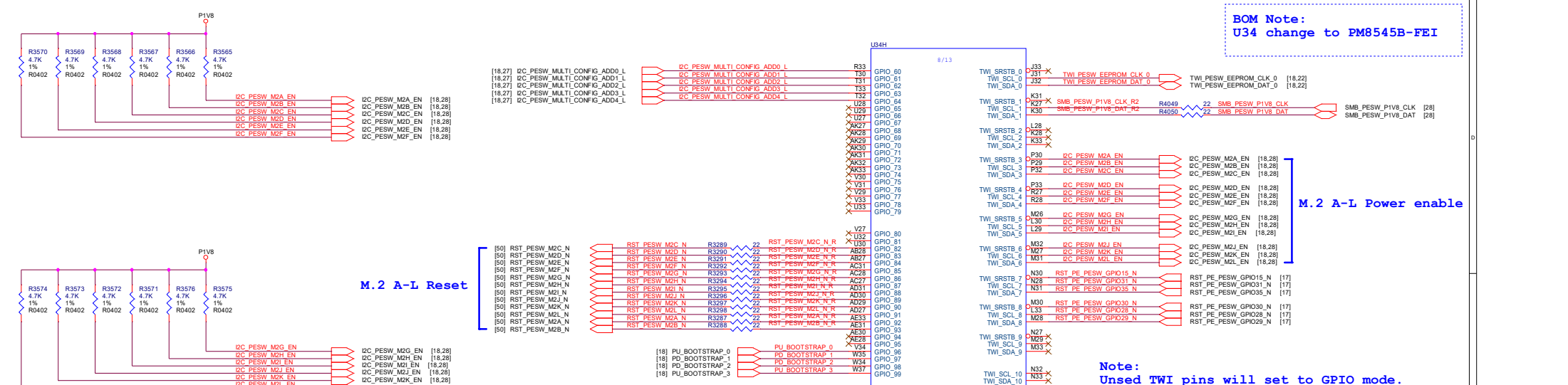
Lane Reversal for layout purpose

Lane Reversal for layout purpose



Stack 6

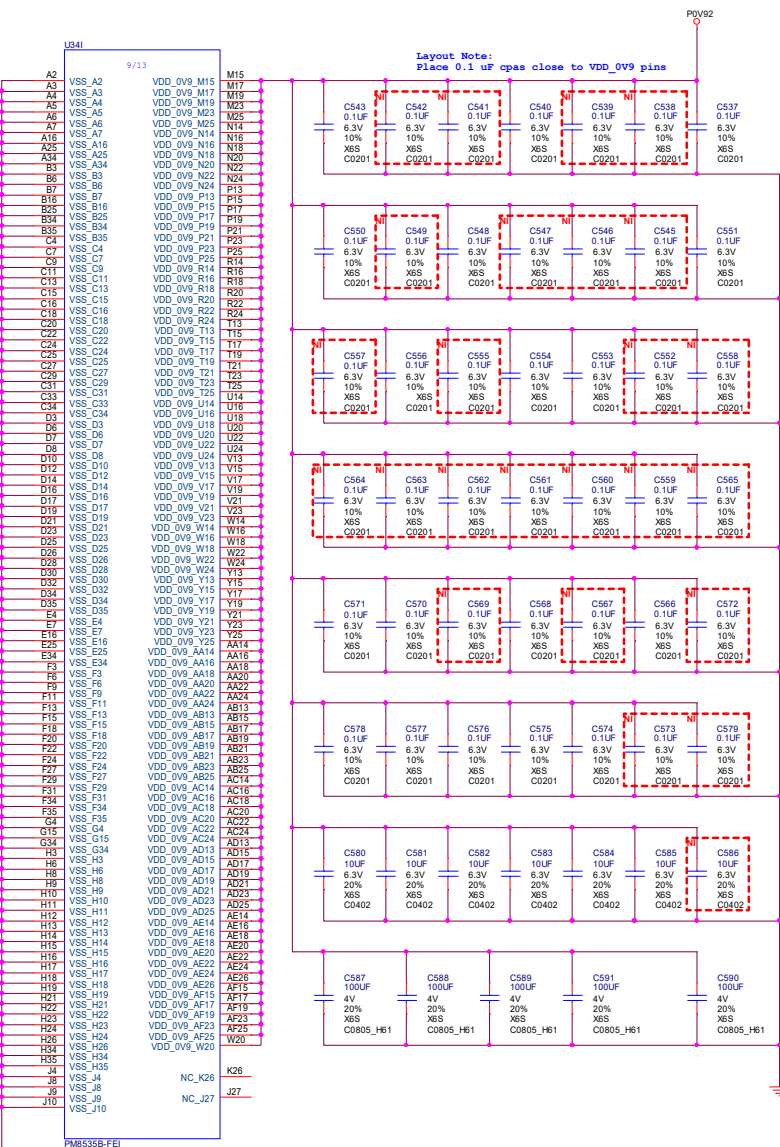




Power Cap

```
GPV2 VDD_0V9
0.1UF-Insert:18/Not Insert:24
4.7UF-0
10UF-Insert 6/Not Insert:1
100UF- Insert:2/Not Insert:3
```

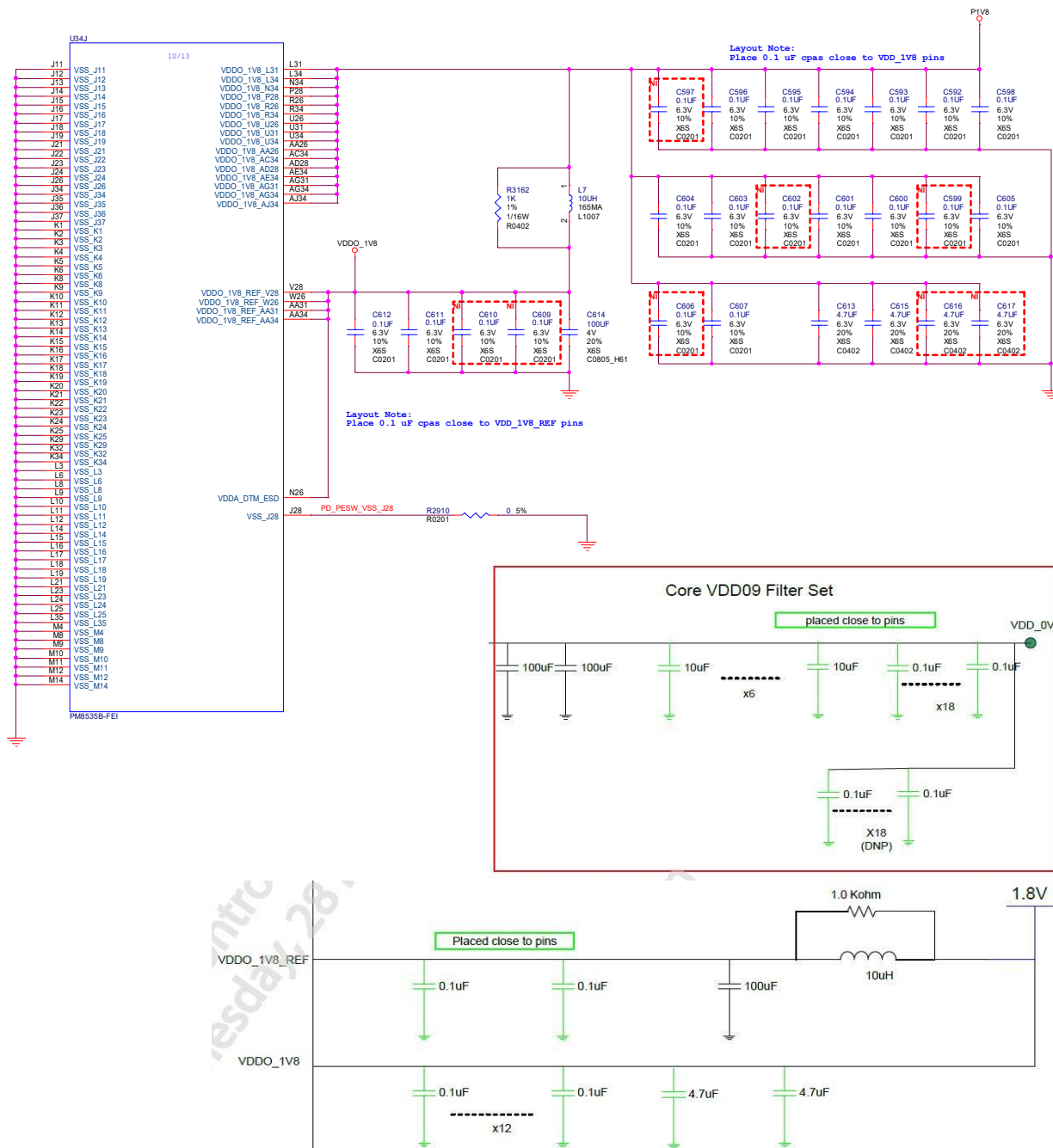
```
SPEC  VDD_OV9
0.1UF-Insert:18/Not Insert:18
4.7UF-0
10UF-Insert:6
100UF-Insert:2
```



Power Cap

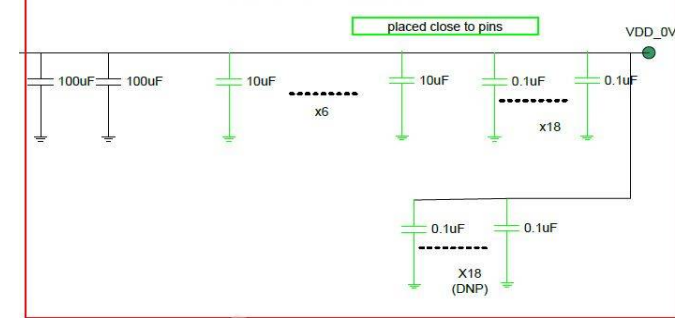
```
GPV2 VDDO_1V8/1V8_REF
0.1UF-Insert:14/Not Insert:6
4.7UF-Insert:2/Not Insert:2
10UF-0
100UF- Insert:1
```

```
SPEC  VDDO_1V8/1V8_REF
0.1UF-Insert:14
4.7UF-Insert:2
10UF-0
100UF-Insert:1
```

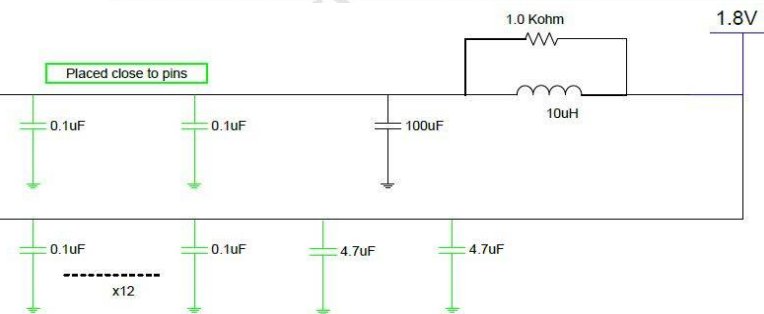


BOM Note:
U34 change to PM8545B-FEI

Core VDD09 Filter Set



Placed close to pins



GFV2_AVD_PCIE_Q/PCIE_TX	SPEC_AVD_PCIE_Q/PCIE_TX
0.1UF-Insert:13/Not Insert:25	0.1UF-Insert:13/Not Insert:1
4.7UF-Insert:2/Not Insert:2	4.7UF-Insert:2
10UF-0	10UF-0
100UF-Insert:1	100UF-Insert:1

BOM Note:
U34 change to PM8545B-FEI



```
0.1UF-Insert:19/Not Insert:22
4.7UF-Insert:12
10UF-0
100UF-Insert:0
```

Note:
AVD_PCIE Power at page 19 is 5X 0.1UF(Insert).
AT page 20 is 14X 0.1UF(Insert)

[illegible]

C684 0.1uF 6.3V 10% X6S C0201	C683 0.1uF 6.3V 10% X6S C0201	C682 0.1uF 6.3V 10% X6S C0201	C680 0.1uF 6.3V 10% X6S C0201	C679 0.1uF 6.3V 10% X6S C0201	C678 0.1uF 6.3V 10% X6S C0201	C677 0.1uF 6.3V 10% X6S C0201	C676 0.1uF 6.3V 10% X6S C0201	C675 0.1uF 6.3V 10% X6S C0201	C681 0.1uF 6.3V 10% X6S C0201
C694 0.1uF 6.3V 10% X6S C0201	C693 0.1uF 6.3V 10% X6S C0201	C692 0.1uF 6.3V 10% X6S C0201	C690 0.1uF 6.3V 10% X6S C0201	C689 0.1uF 6.3V 10% X6S C0201	C688 0.1uF 6.3V 10% X6S C0201	C687 0.1uF 6.3V 10% X6S C0201	C686 0.1uF 6.3V 10% X6S C0201	C685 0.1uF 6.3V 10% X6S C0201	C691 0.1uF 6.3V 10% X6S C0201

[illegible]

Layout Note:
Place 0.1 uF cpas close to AVD_PCIE pins

C667	C668	C669	C670
4.7UF	4.7UF	4.7UF	4.7UF
6.3V	6.3V	6.3V	6.3V
20%	20%	20%	20%
X6S	X6S	X6S	X6S
C0402	C0402	C0402	C0402

C749	C750	C751	C752
4.7UF	4.7UF	4.7UF	4.7UF
6.3V	6.3V	6.3V	6.3V
20%	20%	20%	20%
X6S	X6S	X6S	X6S
C0402	C0402	C0402	C0402

A68	VSS AE8	VSS AK3
A69	VSS AE8	VSS AK6
A70	VSS AE8	VSS AK7
AE10	VSS AE10	VSS AK9
AE11	VSS AE11	VSS AK10
AE12	VSS AE11	VSS AK11
AE13	VSS AE12	VSS AK12
AE14	VSS AE13	VSS AK13
AE15	VSS AE14	VSS AK14
AE16	VSS AE15	VSS AK15
AE17	VSS AE16	VSS AK16
AE18	VSS AE17	VSS AK17
AE19	VSS AE18	VSS AK18
AE20	VSS AE19	VSS AK19
AE21	VSS AE20	VSS AK20
AE22	VSS AE21	VSS AK21
AE23	VSS AE22	VSS AK22
AE24	VSS AE23	VSS AK23
AE25	VSS AE25	VSS AK24
AE26	VSS AE26	VSS AK25
AE27	VSS AE27	VSS AK26
AE28	VSS AE28	VSS AK27
AE29	VSS AE29	VSS AK28
AE30	VSS AE30	VSS AK29
AE31	VSS AE31	VSS AK30
AE32	VSS AE32	VSS AK31
AE33	VSS AE33	VSS AK32
AE34	VSS AE34	VSS AK33
AE35	VSS AE35	VSS AK34
AF8	VSS AF8	VSS AK35
AF9	VSS AF8	VSS AK36
AF10	VSS AF9	VSS AK37
AF11	VSS AF10	VSS AK38
AF12	VSS AF11	VSS AK39
AF13	VSS AF12	VSS AK40
AF14	VSS AF12	VSS AK41
AF15	VSS AF16	VSS AK42
AF16	VSS AF16	VSS AK43
AF17	VSS AF16	VSS AK44
AF18	VSS AF20	VSS AK45
AF19	VSS AF20	VSS AK46
AF20	VSS AF22	VSS AK47
AF21	VSS AF20	VSS AK48
AF22	VSS AF20	VSS AK49
AF23	VSS AF22	VSS AK50
AF24	VSS AF24	VSS AK51
AG3	VSS AG3	VSS AK52
AG4	VSS AG3	VSS AK53
AG5	VSS AG6	VSS AK54
AG6	VSS AG6	VSS AK55
AG7	VSS AG6	VSS AK56
AG8	VSS AG6	VSS AK57
AG9	VSS AG6	VSS AK58
AG10	VSS AG10	VSS AK59
AG11	VSS AG10	VSS AK60
AG12	VSS AG11	VSS AK61
AG13	VSS AG12	VSS AK62
AG14	VSS AG14	VSS AK63
AG15	VSS AG15	VSS AK64
AG16	VSS AG16	VSS AK65
AG17	VSS AG16	VSS AK66
AG18	VSS AG17	VSS AK67
AG19	VSS AG18	VSS AK68
AG20	VSS AG19	VSS AK69
AG21	VSS AG21	VSS AK70
AG22	VSS AG21	VSS AK71
AG23	VSS AG22	VSS AK72
AG24	VSS AG23	VSS AK73
AG25	VSS AG24	VSS AK74
AG26	VSS AG25	VSS AK75
AG27	VSS AG26	VSS AK76
AG28	VSS AG27	VSS AK77
AG29	VSS AG28	VSS AK78
AG30	VSS AG29	VSS AK79
AG31	VSS AG30	VSS AK80
AG32	VSS AG31	VSS AK81
AG33	VSS AG32	VSS AK82
AG34	VSS AG33	VSS AK83
AG35	VSS AG35	VSS AK84
AG36	VSS AG36	VSS AK85
AH2	VSS AH2	VSS AP10
AH3	VSS AH2	VSS AP12
AH4	VSS AH2	VSS AP13
AH5	VSS AH4	VSS AP14
AH6	VSS AH4	VSS AP16
AH7	VSS AH4	VSS AP17
AH8	VSS AH6	VSS AP18
AH9	VSS AH6	VSS AP19
AH10	VSS AH8	VSS AP21
AH11	VSS AH8	VSS AP23
AH12	VSS AH10	VSS AP24
AH13	VSS AH11	VSS AP25
AH14	VSS AH12	VSS AP26
AH15	VSS AH13	VSS AP27
AH16	VSS AH14	VSS AP28
AH17	VSS AH15	VSS AP29
AH18	VSS AH16	VSS AP30
AH19	VSS AH17	VSS AP31
AH20	VSS AH18	VSS AP32
AH21	VSS AH19	VSS AP33
AH22	VSS AH21	VSS AP34
AH23	VSS AH22	VSS AP35
AH24	VSS AH23	VSS AP36
AH25	VSS AH24	VSS AP37
AH26	VSS AH25	VSS AP38
AH27	VSS AH26	VSS AP39
AH28	VSS AH27	VSS AP40
AH29	VSS AH28	VSS AP41
AH30	VSS AH29	VSS AP42
AH31	VSS AH30	VSS AP43
AH32	VSS AH31	VSS AP44
AH33	VSS AH32	VSS AP45
AH34	VSS AH33	VSS AP46
AJ4	VSS AJ4	VSS AR1
AJ8	VSS AJ8	VSS AR2
AJ9	VSS AJ8	VSS AR3
AJ10	VSS AJ9	VSS AR4
AJ11	VSS AJ10	VSS AR5
AJ12	VSS AJ11	VSS AR6
AJ13	VSS AJ12	VSS AR7
AJ14	VSS AJ13	VSS AR8
AJ15	VSS AJ14	VSS AR9
AJ16	VSS AJ15	VSS AR10
AJ17	VSS AJ16	VSS AR11
AJ18	VSS AJ17	VSS AR12
AJ19	VSS AJ18	VSS AR13
AJ20	VSS AJ19	VSS AR14
AJ21	VSS AJ20	VSS AR15
AJ22	VSS AJ21	VSS AR16
AJ23	VSS AJ22	VSS AR17
AJ24	VSS AJ23	VSS AR18
AJ25	VSS AJ24	VSS AR19
AJ26	VSS AJ25	VSS AR20
AJ27	VSS AJ26	VSS AR21
AJ28	VSS AJ27	VSS AR22
AJ29	VSS AJ28	VSS AR23
AJ30	VSS AJ29	VSS AR24
AJ31	VSS AJ30	VSS AR25
AJ32	VSS AJ31</	

The diagram illustrates the placement of decoupling capacitors on the AVD power planes. It is divided into three horizontal sections corresponding to different voltage rails: AVD_0V9, AVD_PCIE, and AVD_0V5.

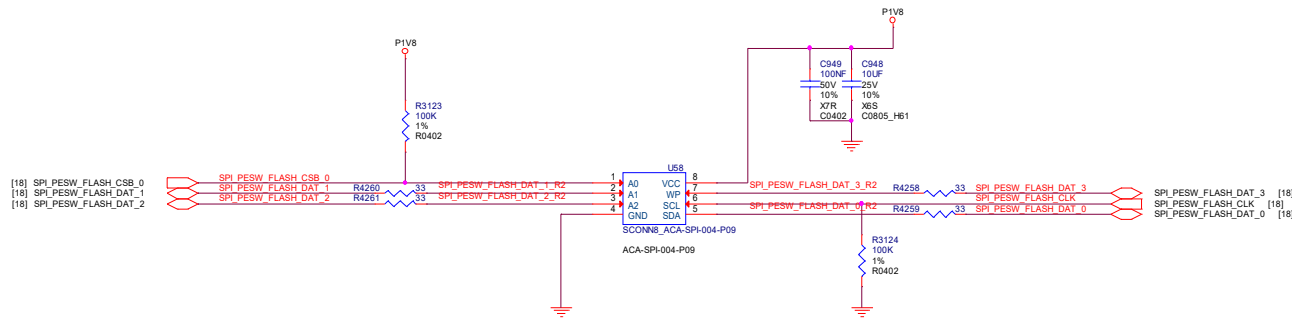
- AVD_0V9 Section:** A horizontal bus is shown with a label "Placed close to pins" in a green box. Capacitors are placed at regular intervals along the bus:
 - 0.1uF capacitors (x6) are placed near the pins.
 - 4.7uF capacitors (x4) are placed further along the bus.
 - 0.1uF capacitors (x5 (DNP)) are placed near the end of the bus.
- AVD_PCIE Section:** A horizontal bus is shown with a label "Placed at each vco power pins". Four 0.1uF capacitors are placed at regular intervals along the bus.
- AVD_0V5 Section:** A horizontal bus is shown with a label "Placed at each vco power pins". Capacitors are placed at regular intervals along the bus:
 - 0.1uF capacitors (x8) are placed near the pins.
 - 4.7uF capacitors (x8) are placed further along the bus.
 - 0.1uF capacitors (x8 (DNP)) are placed near the end of the bus.

A 1.0 Kohm resistor is shown at the bottom right, connected to the AVD_0V5 rail. The diagram also includes a watermark "of Quantia on" and a timestamp "06 PM".

Quanta	Department CCBU	Designer Reviewer	<Designer> <Reviewer>	Project Glacier Point V2	Doc Number <Doc> Page Title PCIE SWITCH (PWR3/VSS3)	Rev 3.02
				Size C Date: Thursday, November 12, 2020	Sheet 21 of 67	

Note:
SPI Flash is W25Q128FWSIQ.

SPI flash socket



Serial EEPROM 128kb

TWI Address: 0xA0

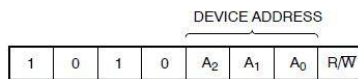
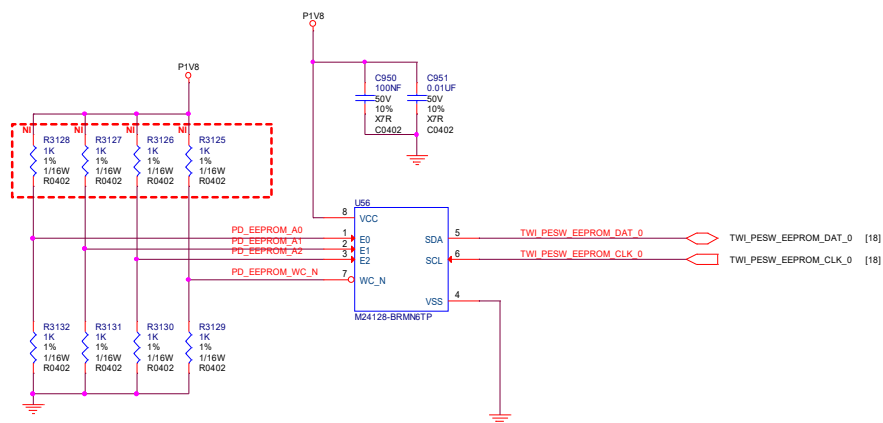
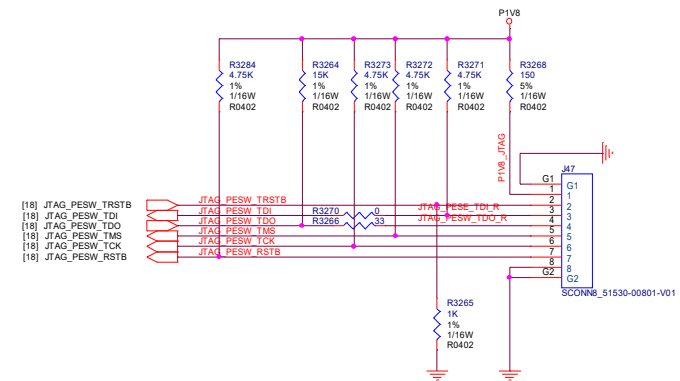
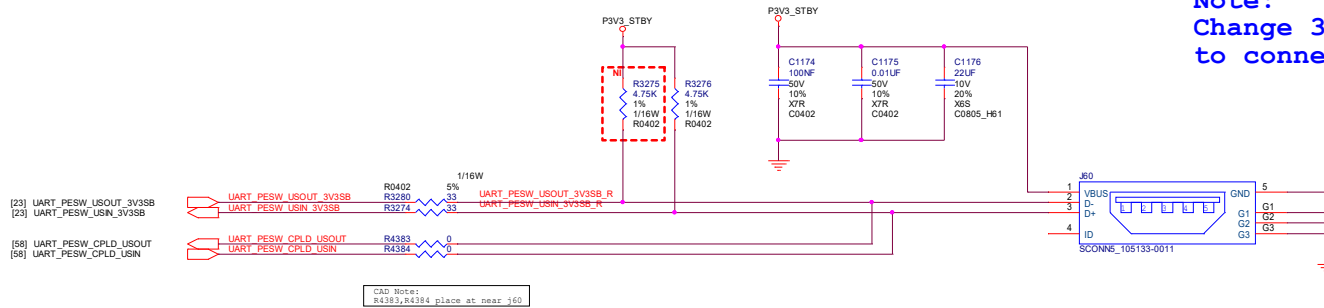


Figure 3. Slave Address Bits

JTAG

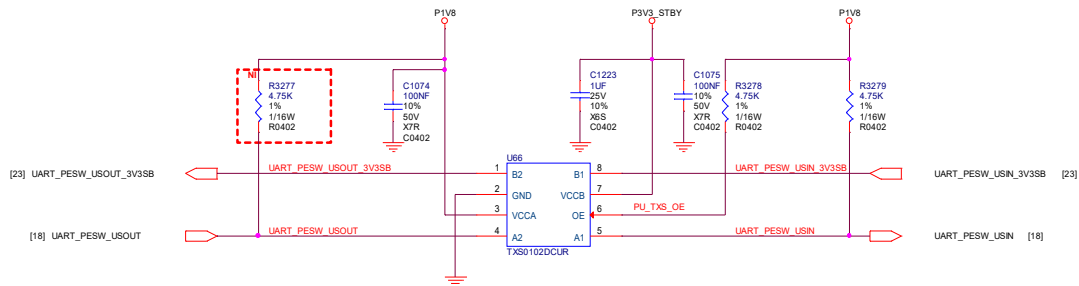


UART 3-PIN HEADER



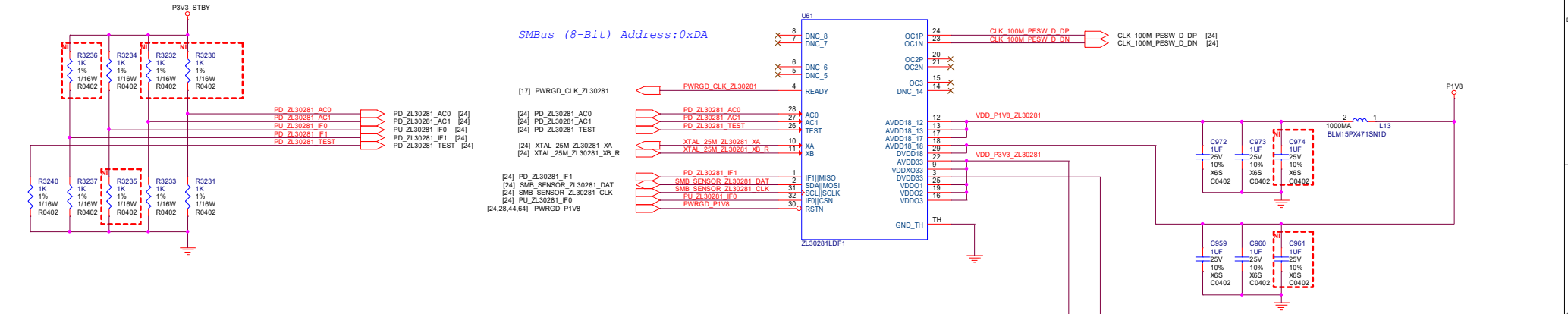
Note:
Change 3 pin header to micro USB
to connect to debug board

LEVEL SHIFTER (1.8V TO 3.3V STBY)

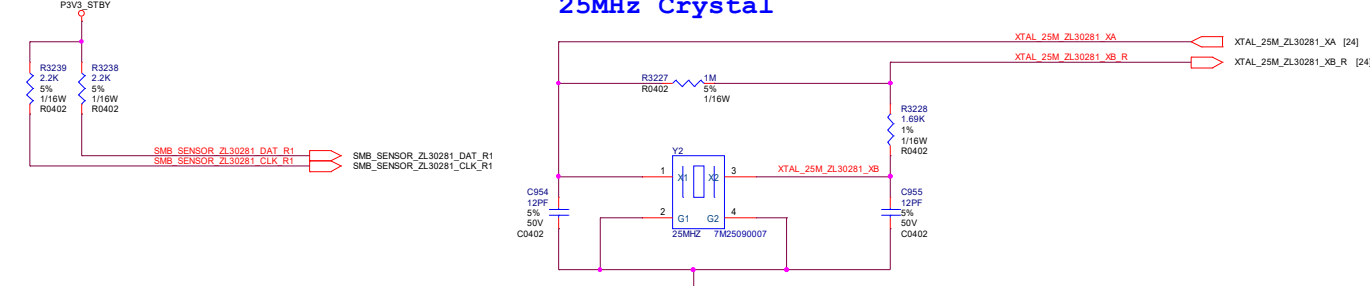


AC1	AC0	Auto Configuration
0	0	Config0: 100MHz on OC1 (CML signal format)
0	1	Config1: 100MHz on OC1 and OC2 (CML)
1	0	Config2: 100MHz on OC1 (CML) and OC2 (HSTL format)
1	1	Config3: 100MHz on OC1 and OC2 (CML) and 25MHz LVCMOS on OC3

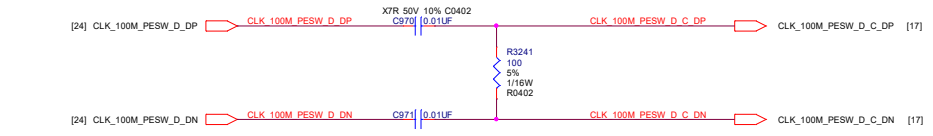
IF1	IF0	Processor Interface
0	0	I ² C, slave address 11011 00
0	1	I ² C, slave address 11011 01
1	0	I ² C, slave address 11011 10
1	1	SPI Slave



25MHz Crystal

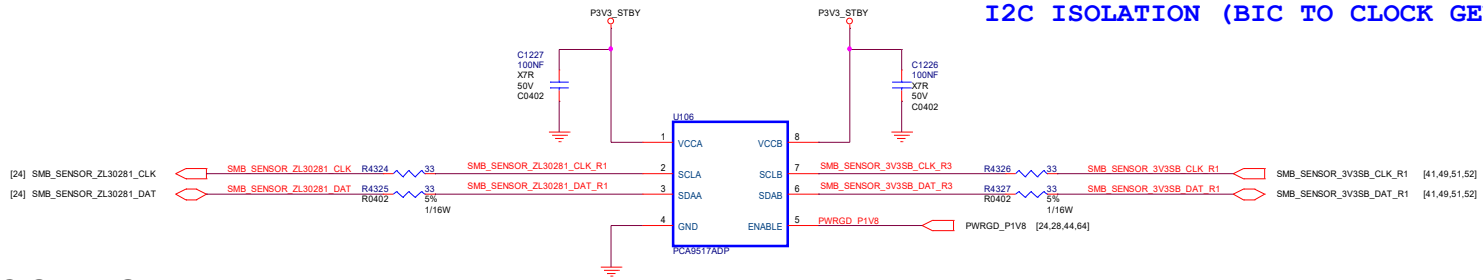


Termination (CML to LVDS)



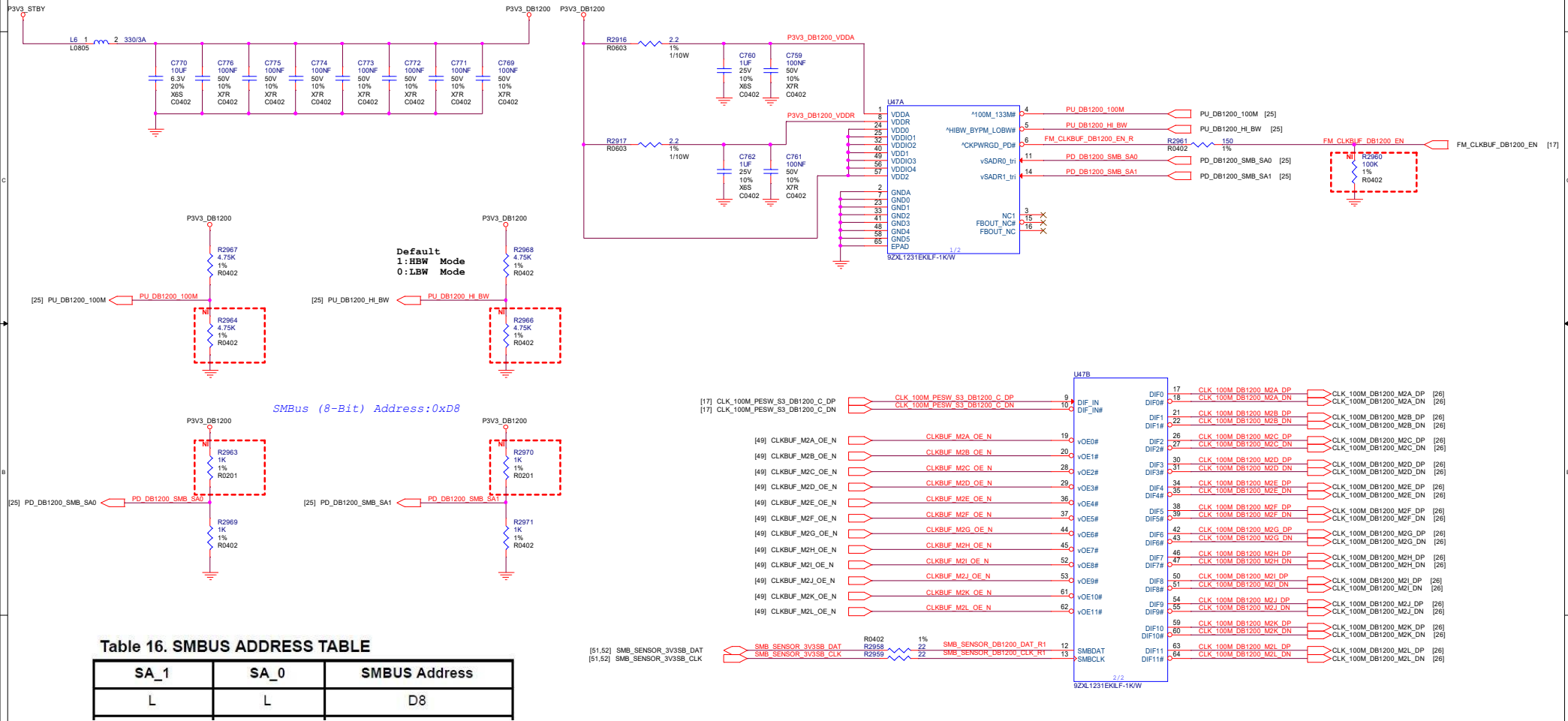
Note: R3241 place close to the input pins of PM8545

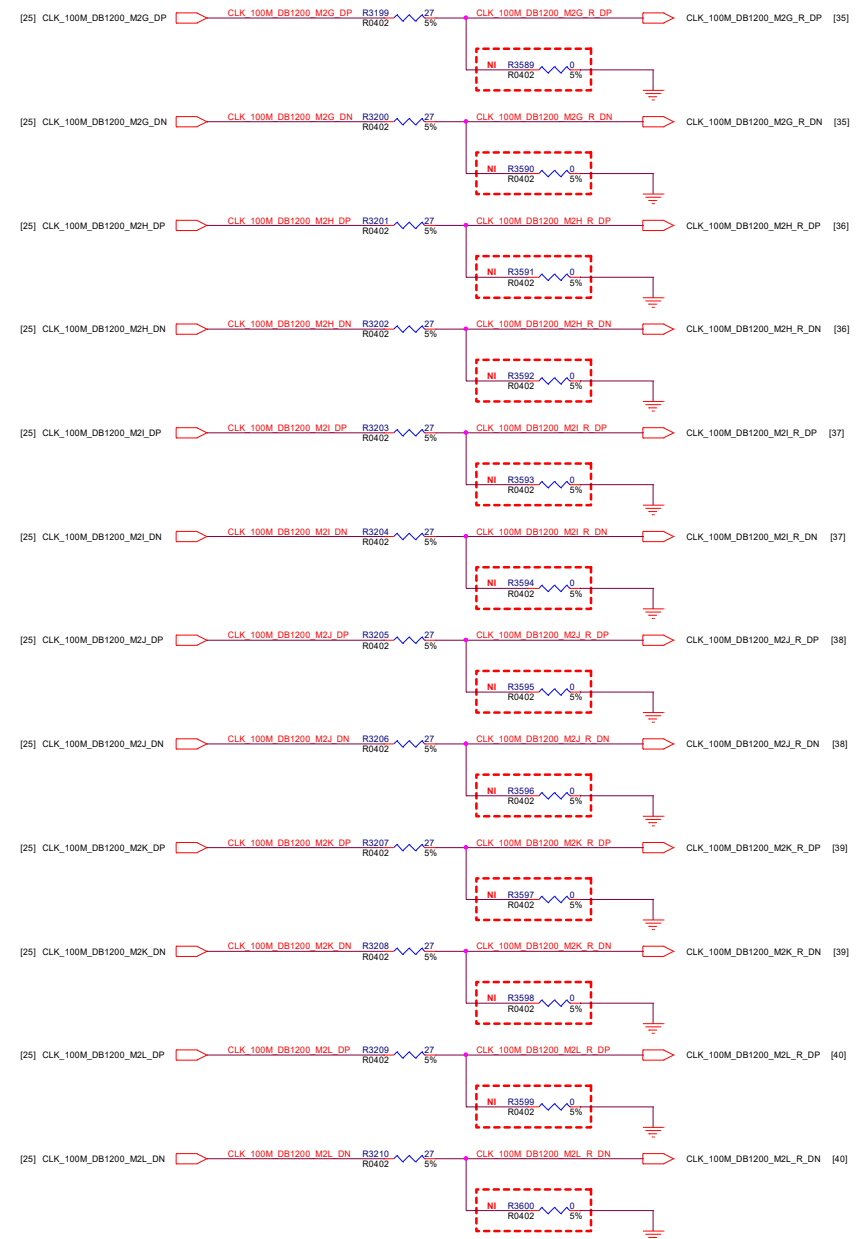
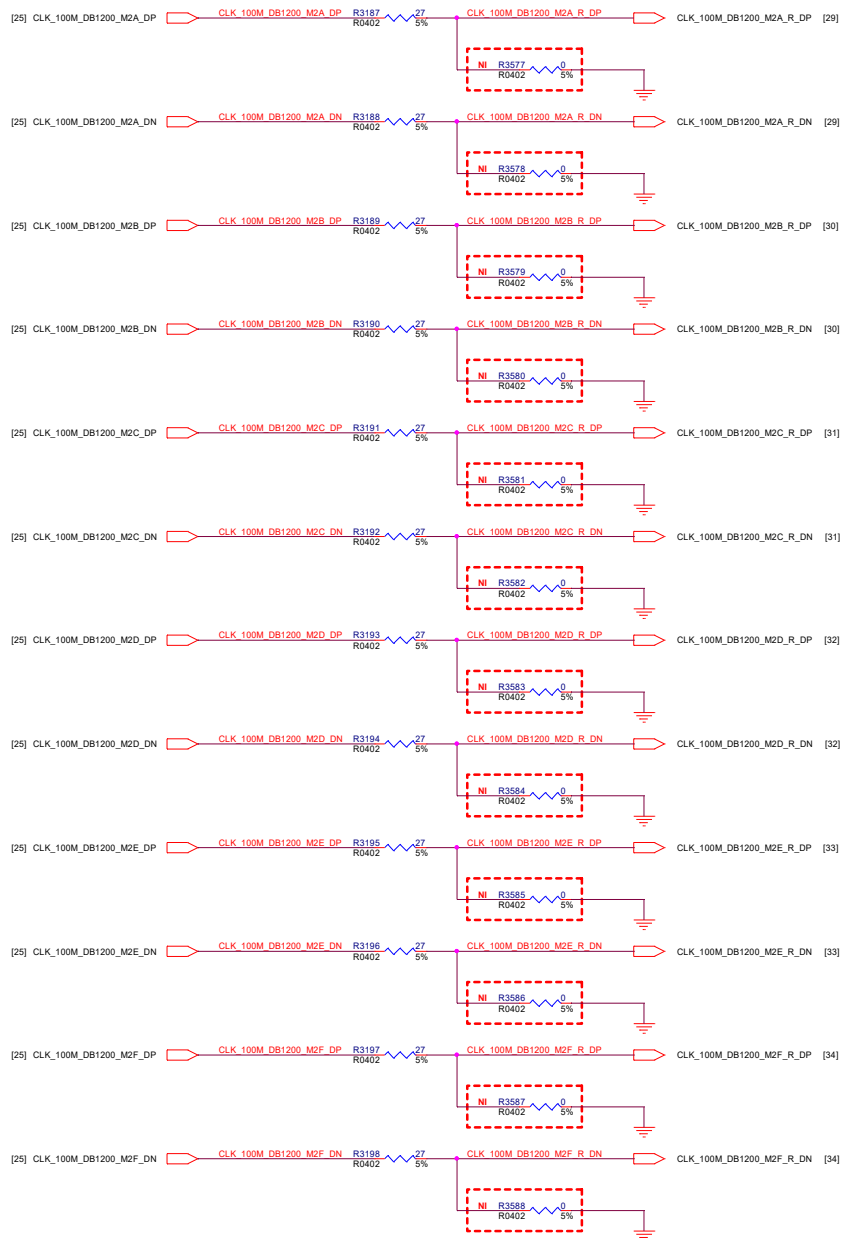
I2C ISOLATION (BIC TO CLOCK GEN)



100MHz CLOCK GEN

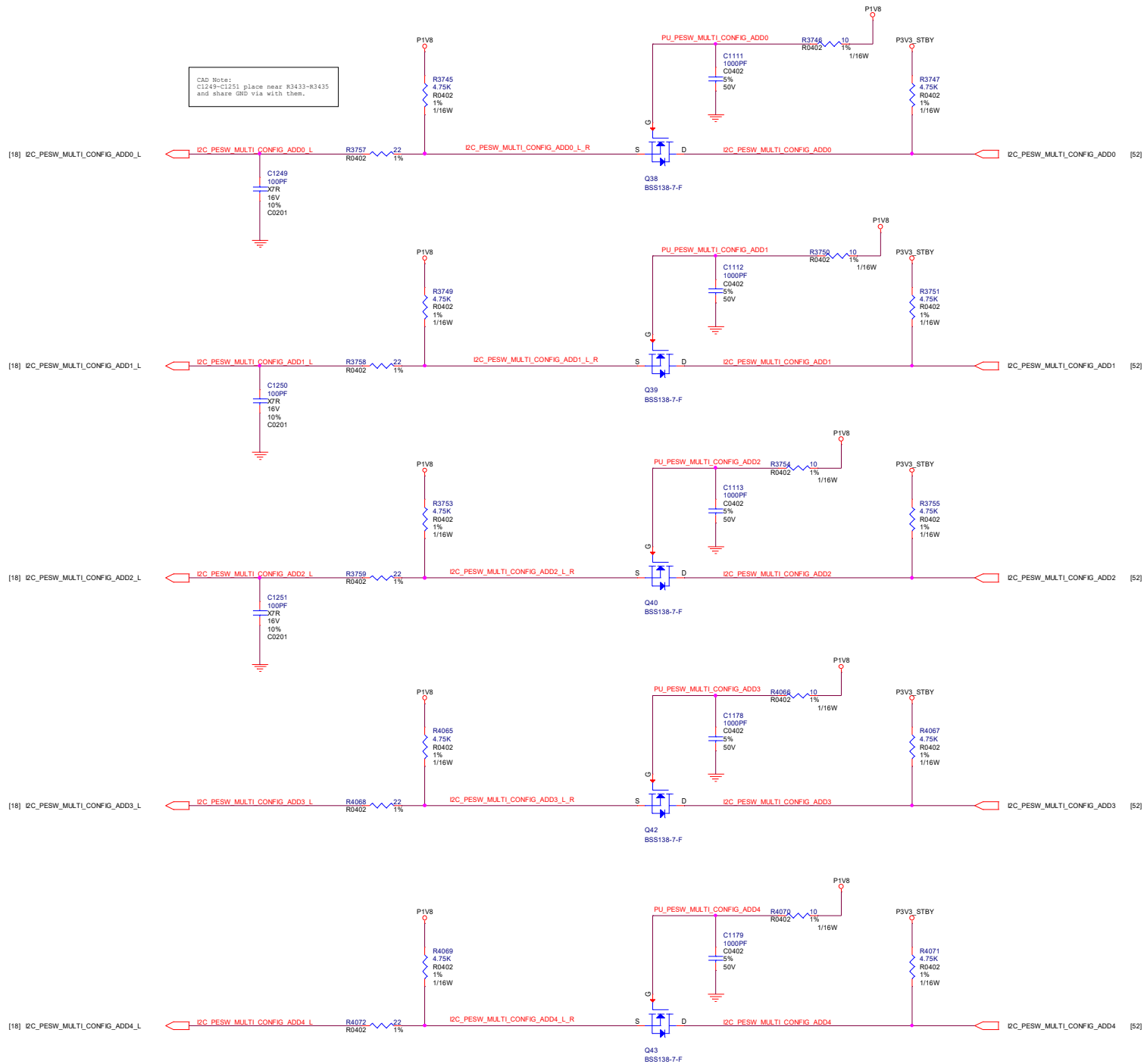
PCIE CLOCK BUFFER





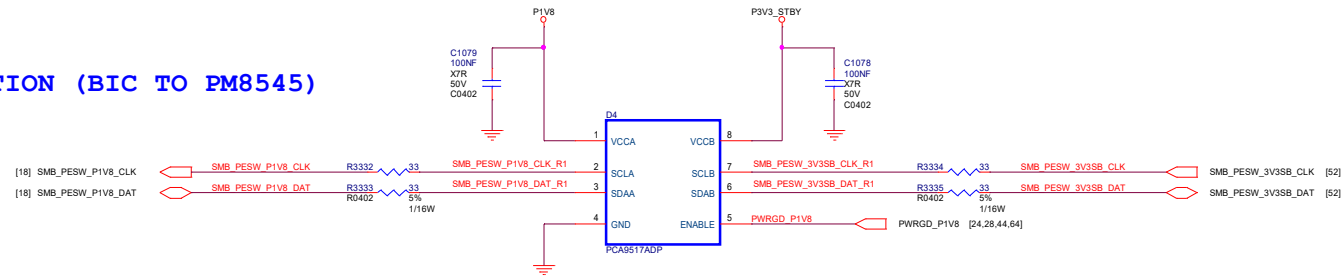
CLOCK BUFFER 2

CAD Note:
C1249-C1251 place near R3433-R3435
and share GND via with them.

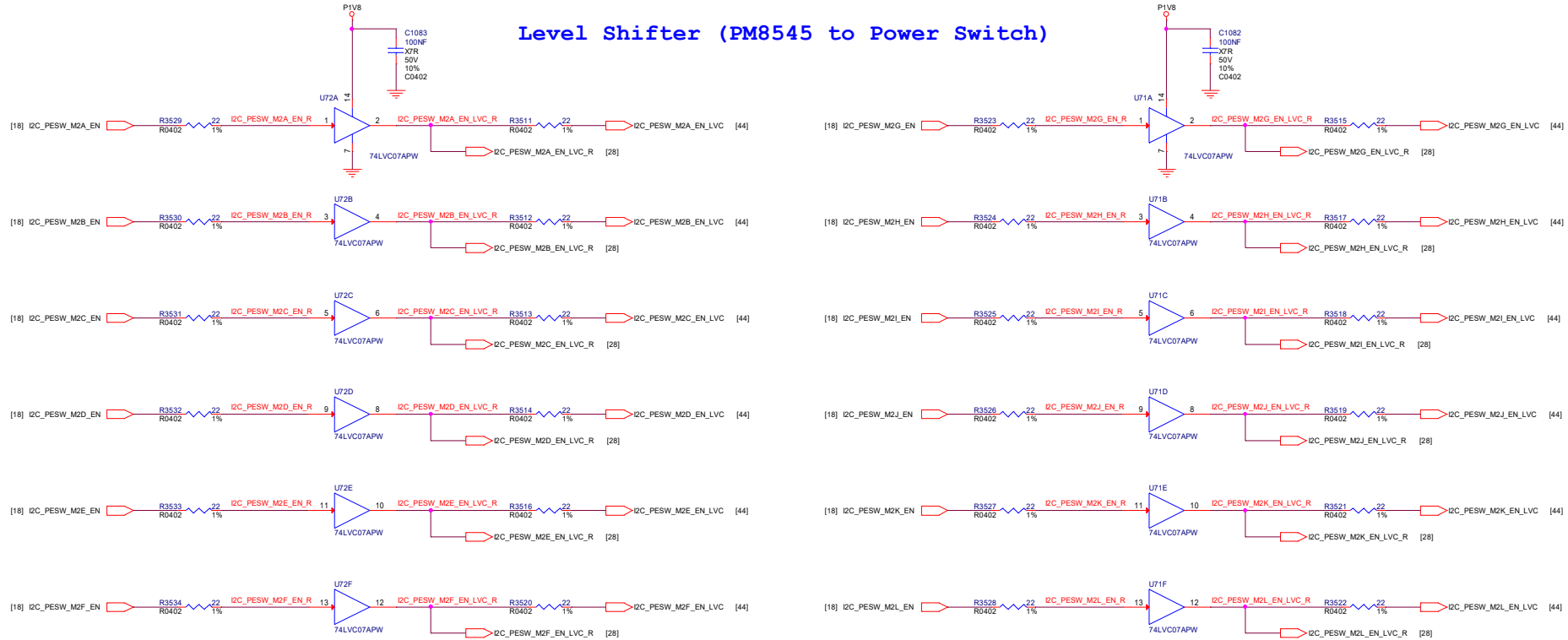


LEVEL SHIFTER 1

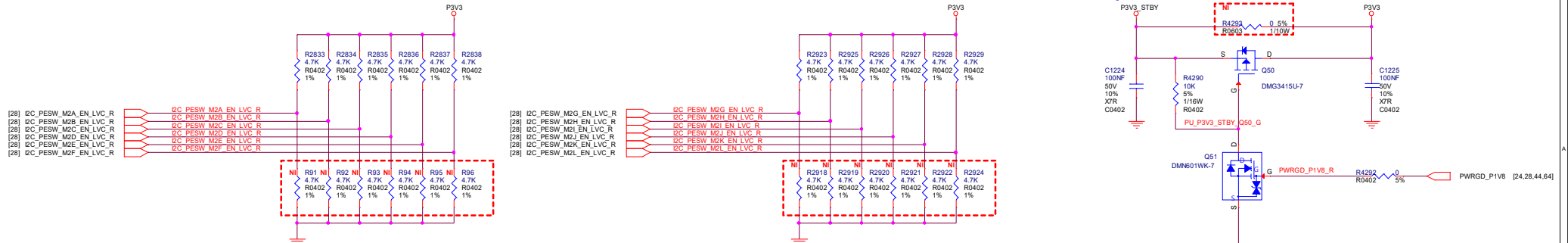
I2C ISOLATION (BIC TO PM8545)

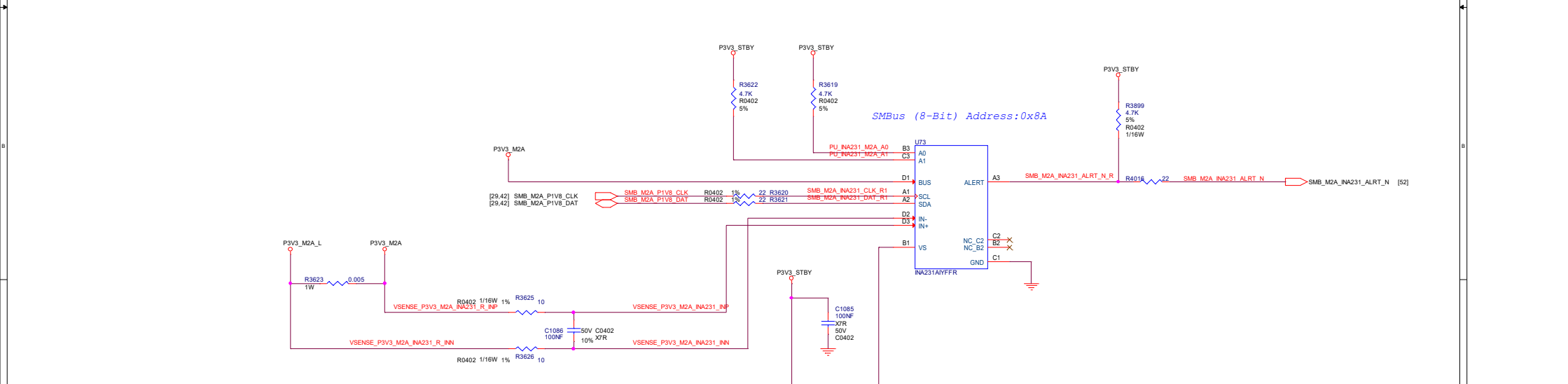


Level Shifter (PM8545 to Power Switch)

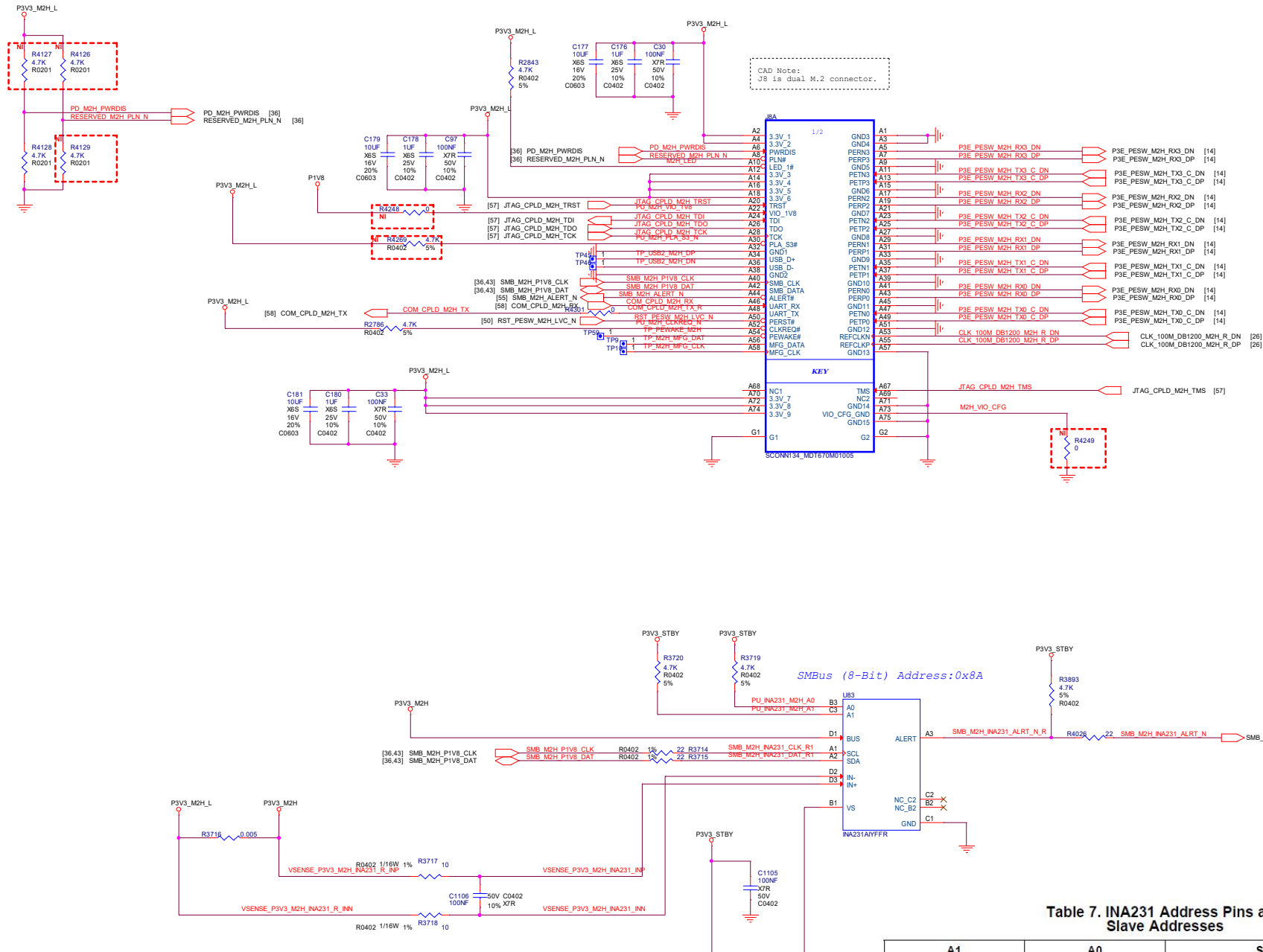


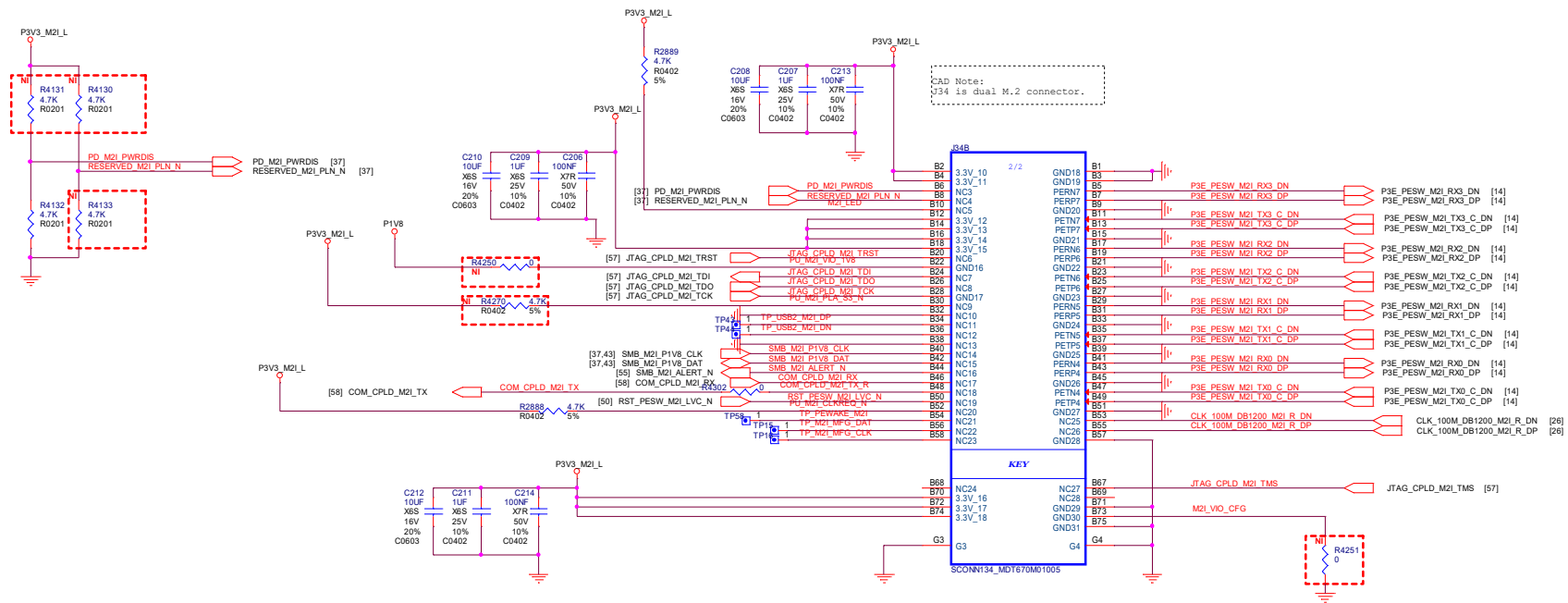
Note: Using P3V3 normal power to avoid unexpected output when VCC is 0V.





A1	A0	SLAVE ADDRESS
V _S	V _S	1000101





SMBus (8-Bit) Address: 0x8A

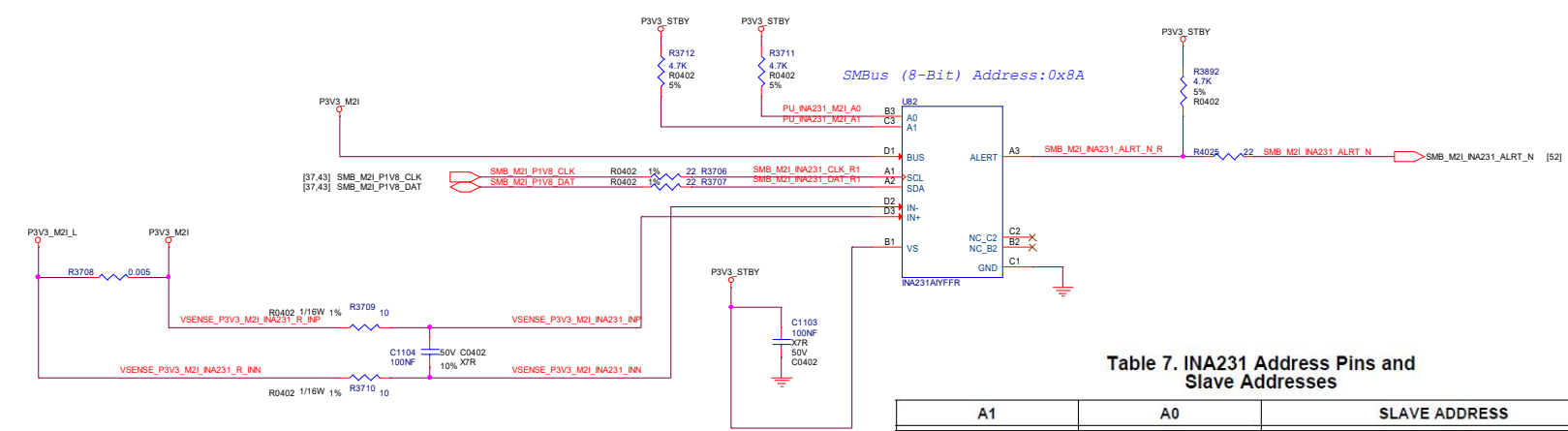
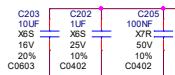
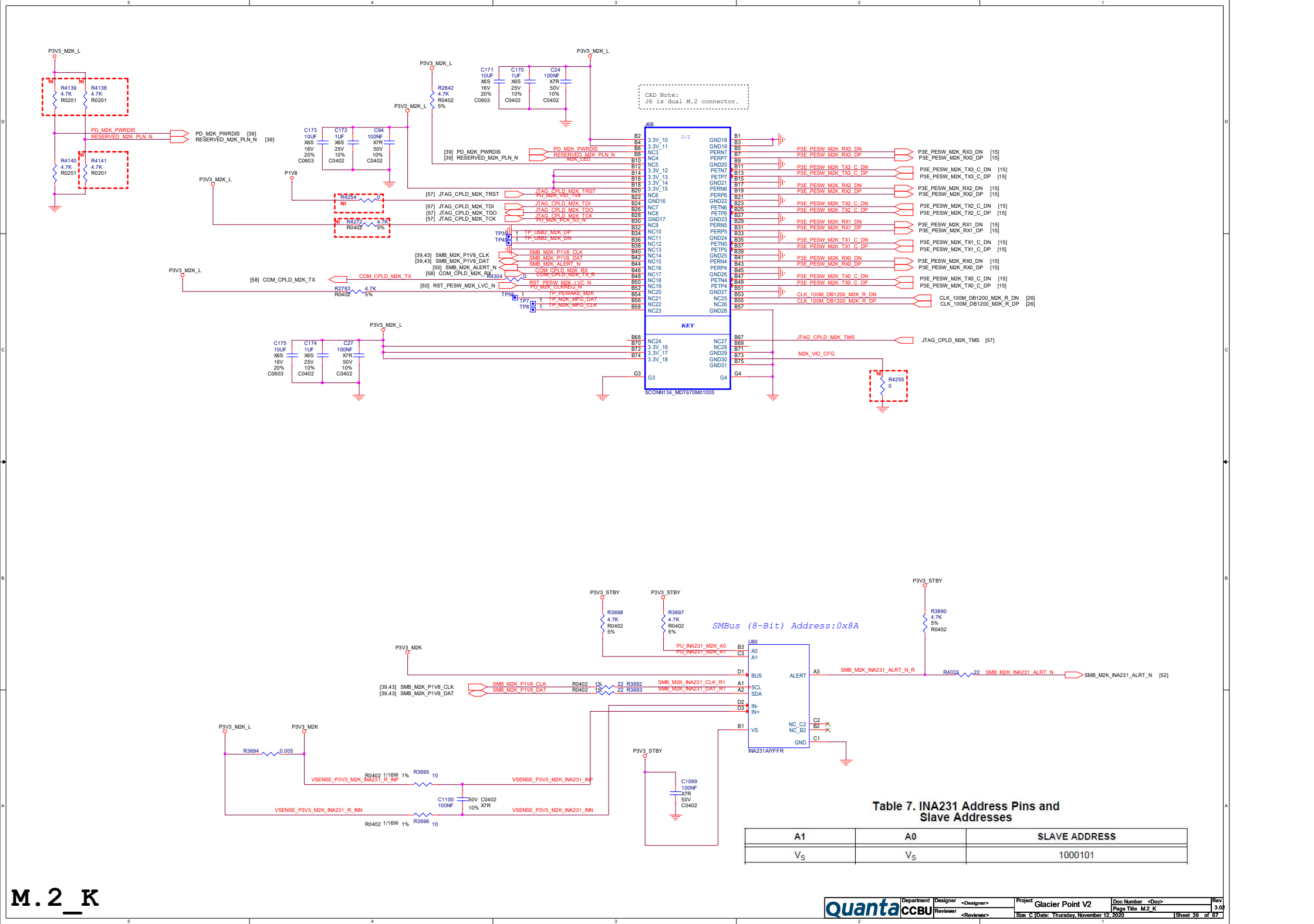


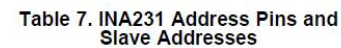
Table 7. INA231 Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
V _S	V _S	1000101

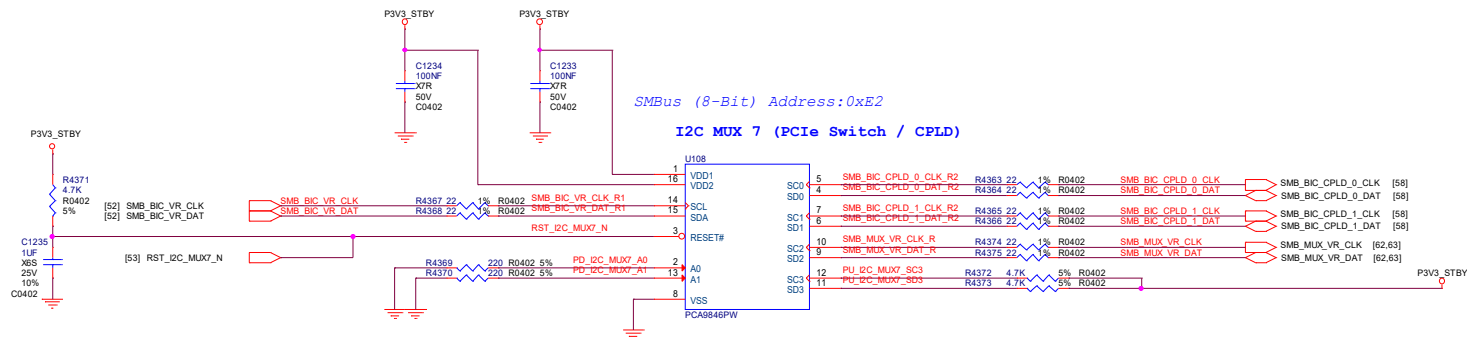
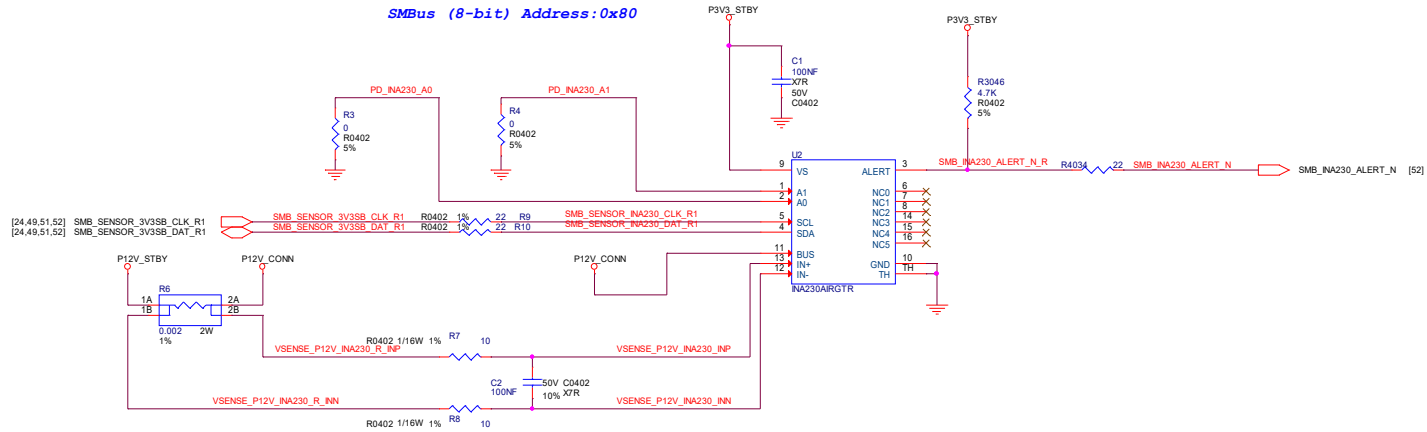


A1	A0	SLAVE ADDRESS
V _S	V _S	1000101





A1	A0	SLAVE ADDRESS
V _S	V _S	1000101



SMB_BIC_CPLD_0_CLK_R2
SMB_BIC_CPLD_0_DAT_R2
SMB_BIC_CPLD_1_CLK_R2
SMB_BIC_CPLD_1_DAT_R2
SMB_MUX_VR_CLK_R
SMB_MUX_VR_DAT_R

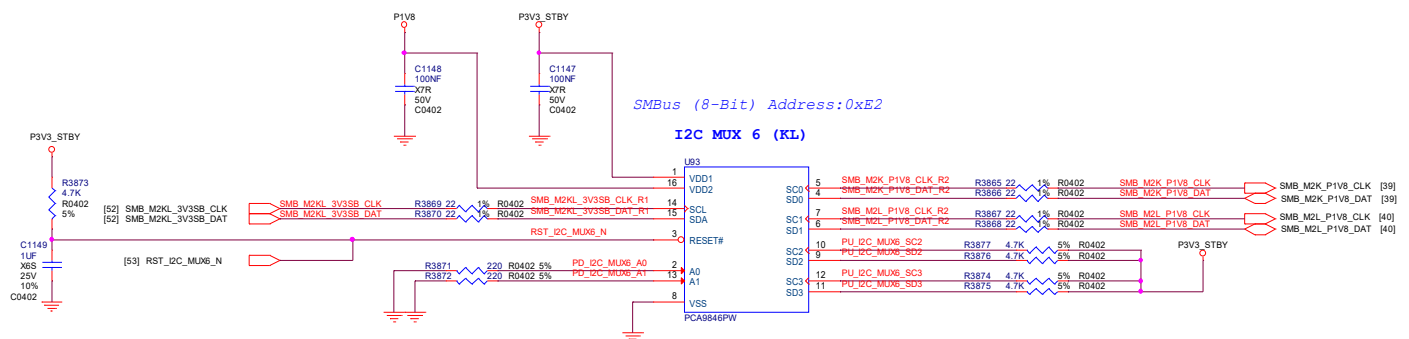
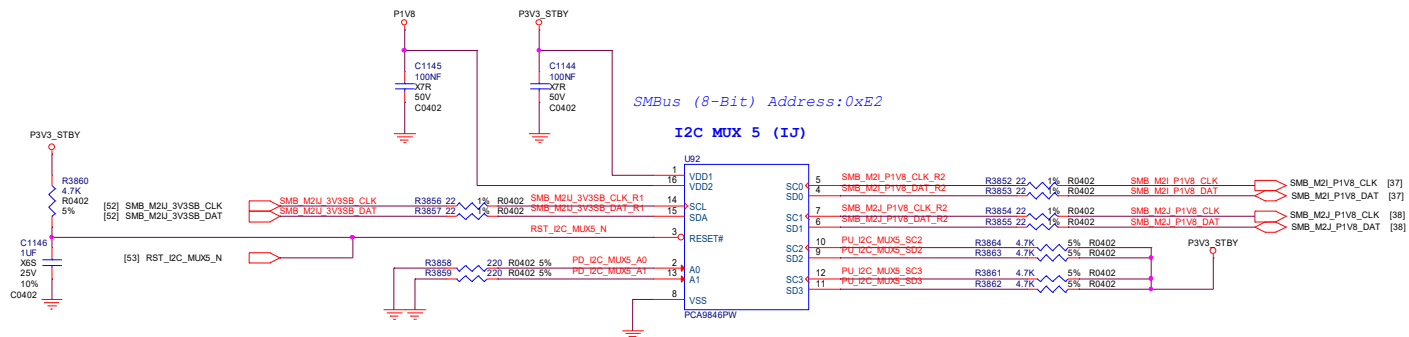
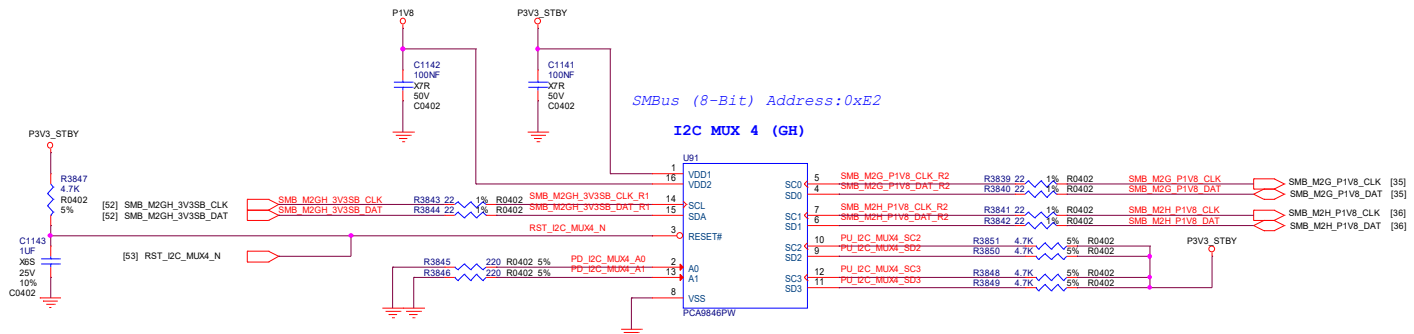
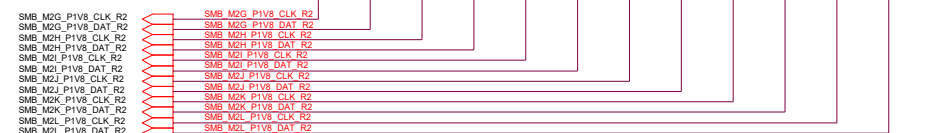


Table 4. Address selection

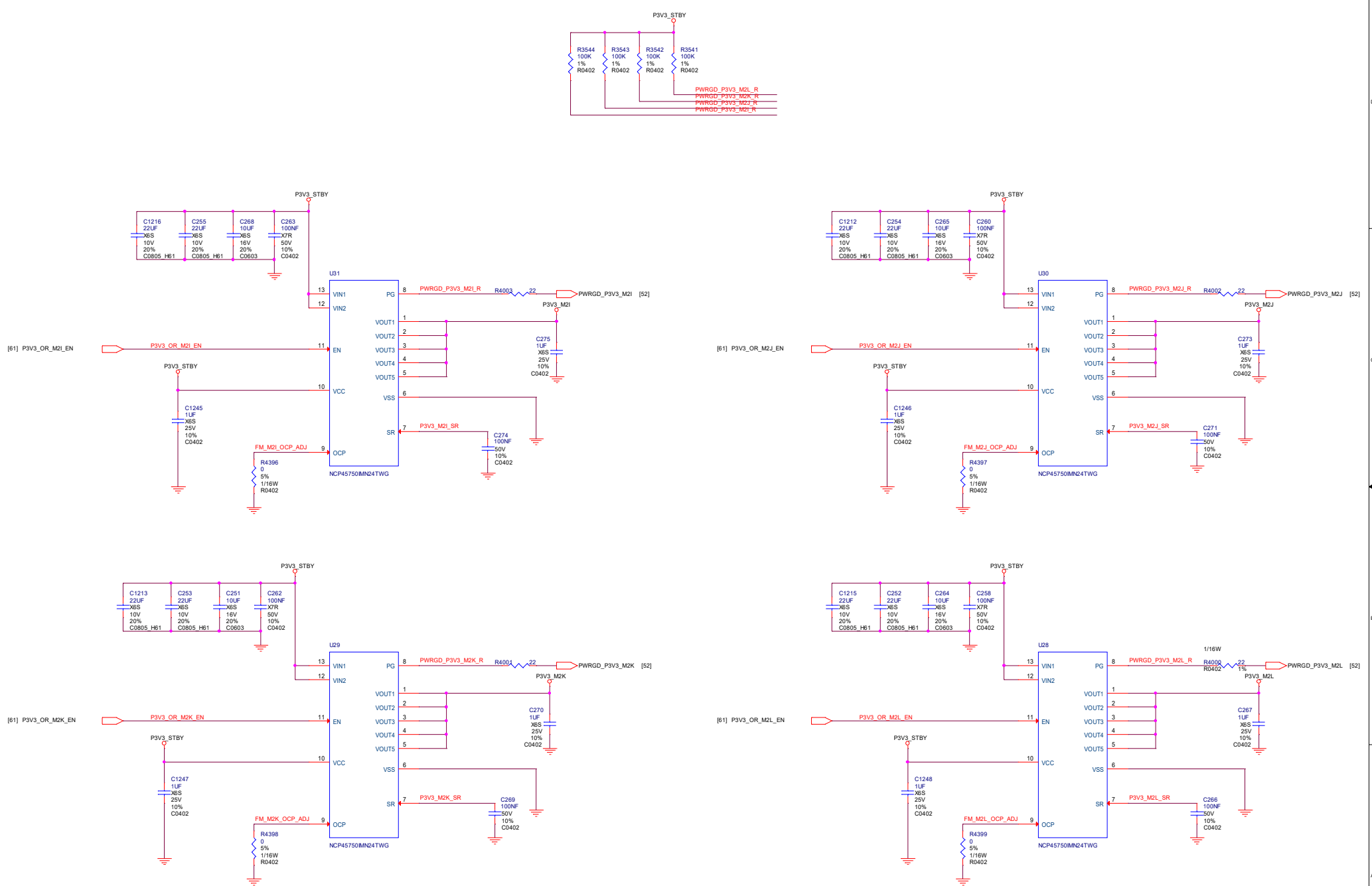
PCA9846 address pins		8-bit I ² C-bus address	Slave address/bit pattern master must send							
A1	A0		A7	A6	A5	A4	A3	A2	A1	A0 - R/W
0	SCL	0xE0h	1	1	1	0	0	0	0	0/1
0	0	0xE2h	1	1	1	0	0	0	1	0/1



I2C MUX 4-6

P3V3 M.2 SWITCH 3

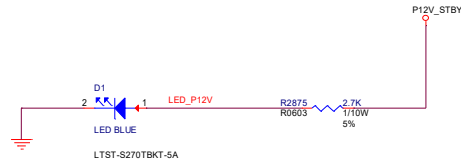
P3V3 M.2 SWITCH 4



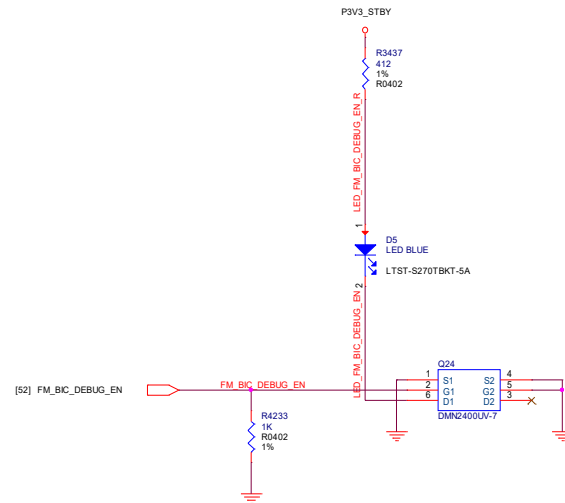
P12V LED

LAYOUT NOTE:

Add SilkScreen "P12V_STBY" next to the LED



BIC_DEBUG_EN LED



All LEDs have to be placed along top edge of the card

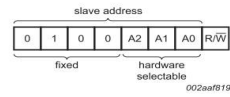
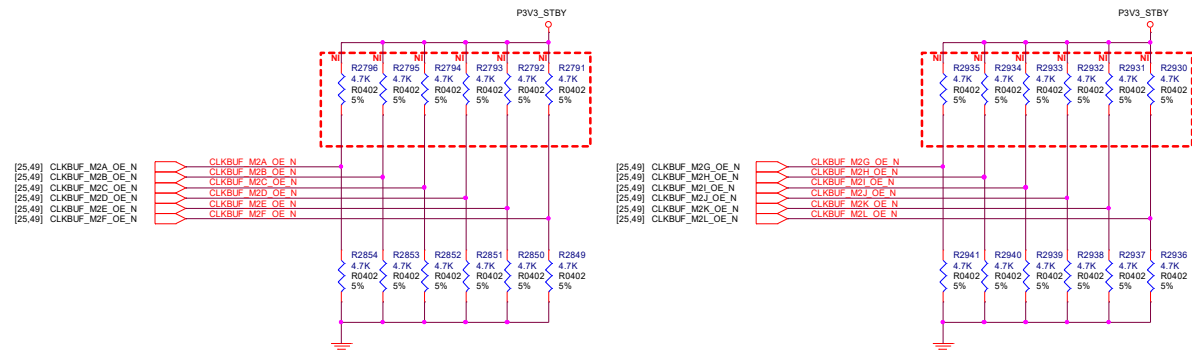
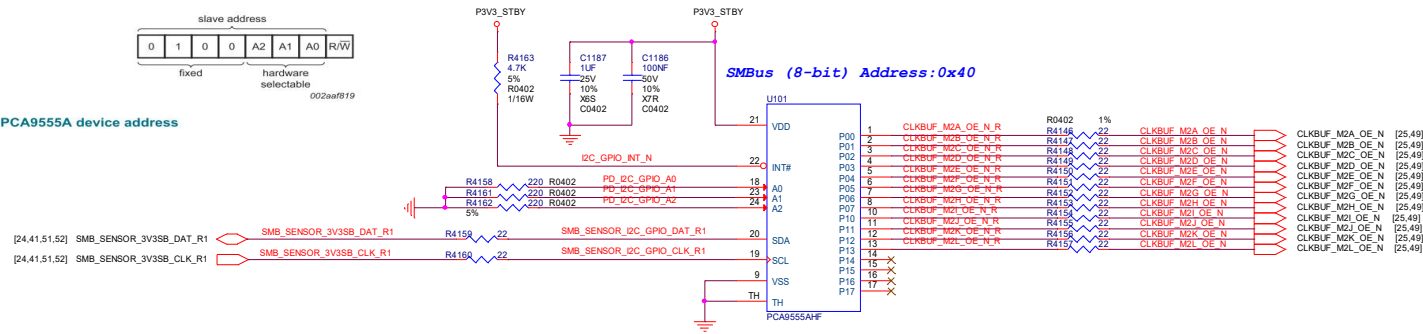
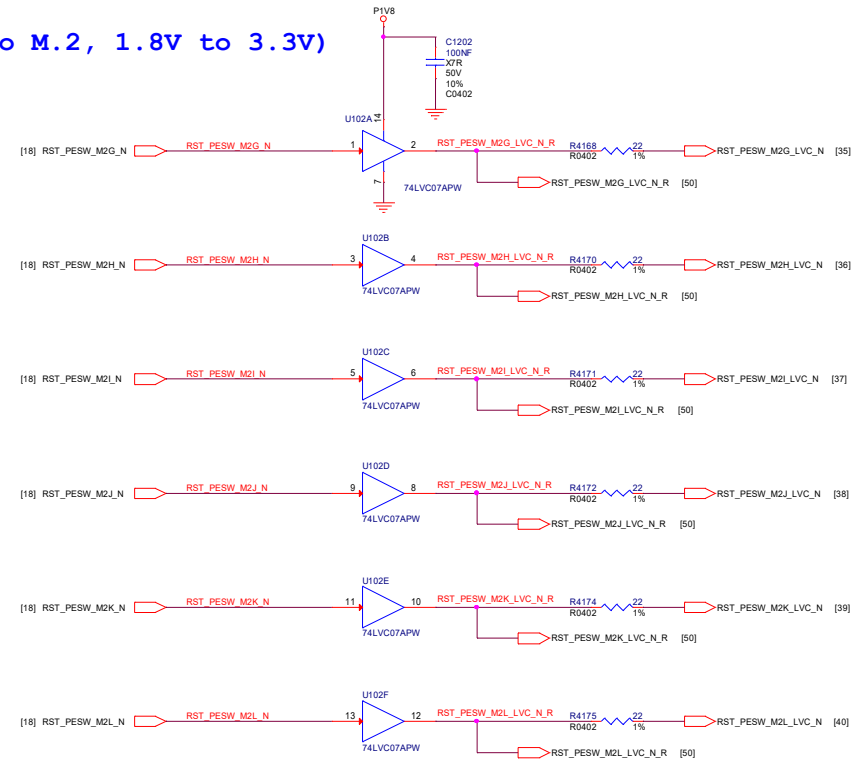


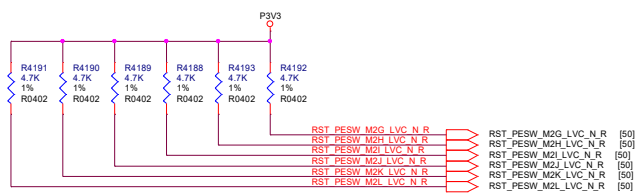
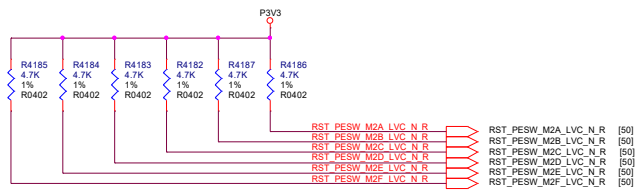
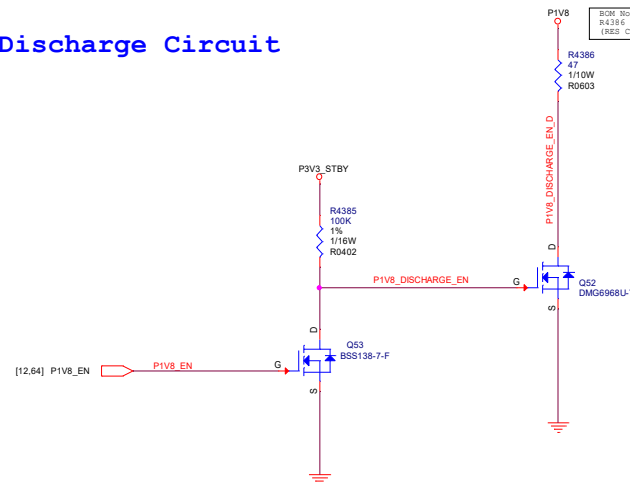
Fig 4. PCA9555A device address



Level Shifter (PM8545 to M.2, 1.8V to 3.3V)



Discharge Circuit



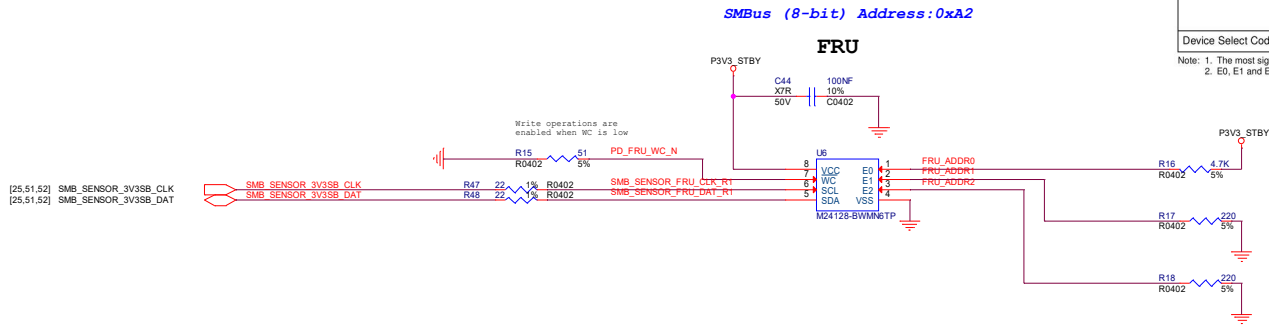


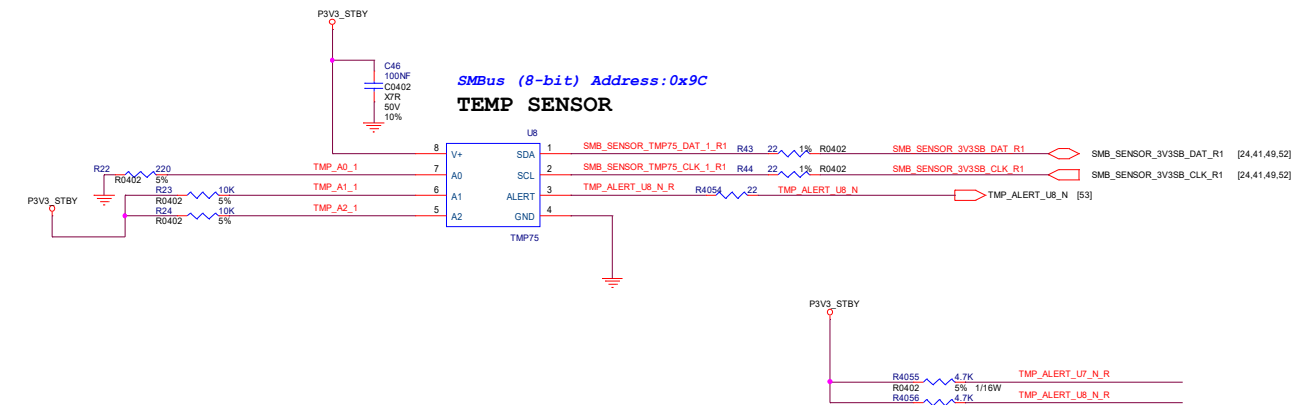
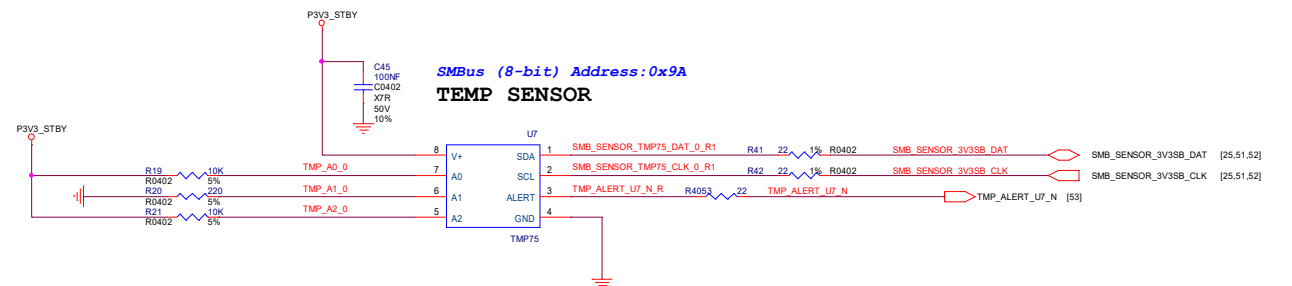
Table 2. Device Select Code

Device Select Code	Device Type Identifier ¹				Chip Enable Address ²			RW
	b7	b6	b5	b4	b3	b2	b1	b0
	1	0	1	0	E2	E1	E0	RW

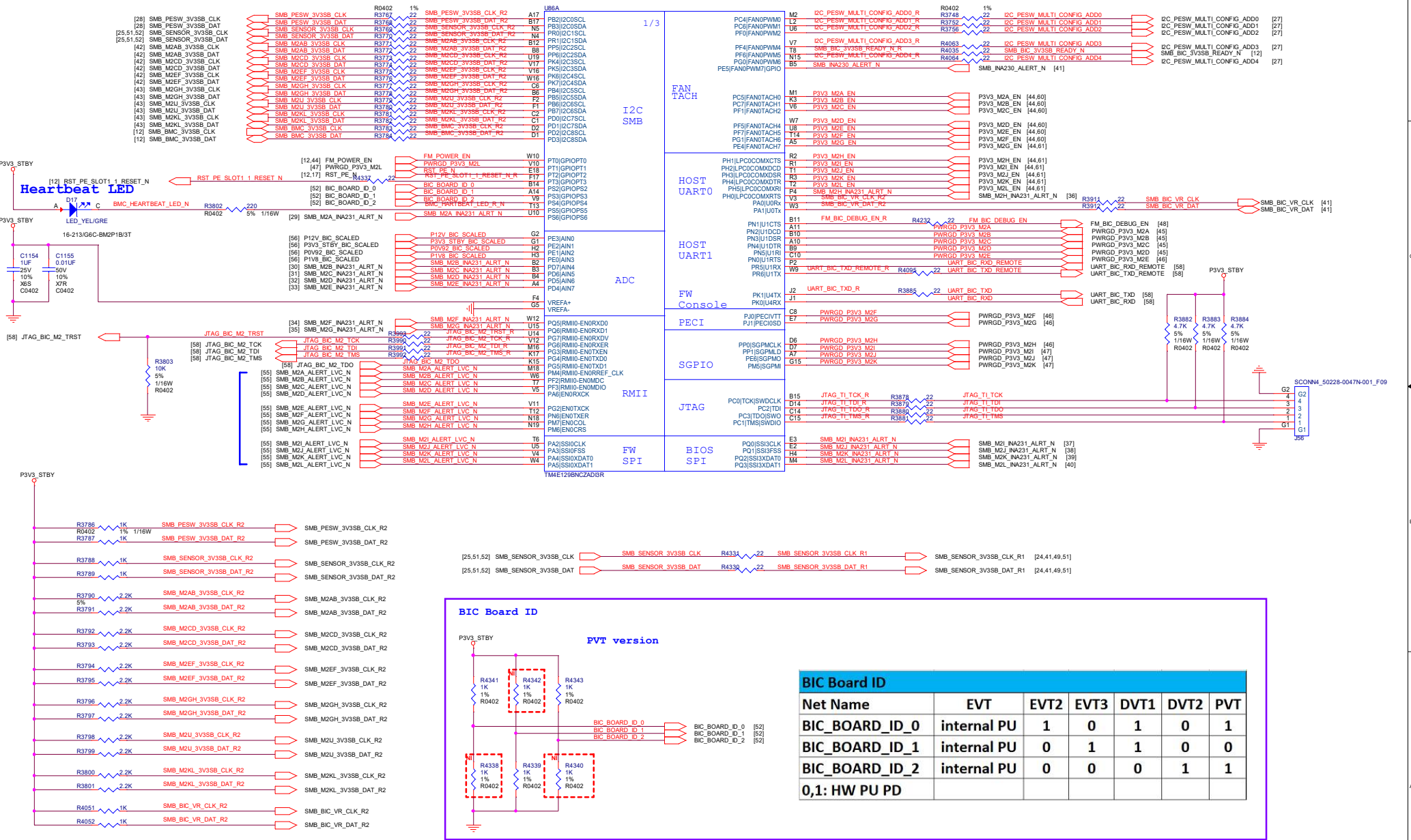
Note: 1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.

A2	A1	A0	SLAVE ADDRESS
0	0	0	1001000
0	0	1	1001001
0	1	0	1001010
0	1	1	1001011
1	0	0	1001100
1	0	1	1001101
1	1	0	1001110
1	1	1	1001111

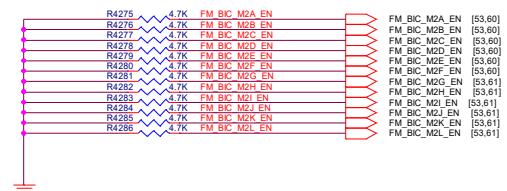
Table 12. Address Pins and Slave Addresses for the TMP75

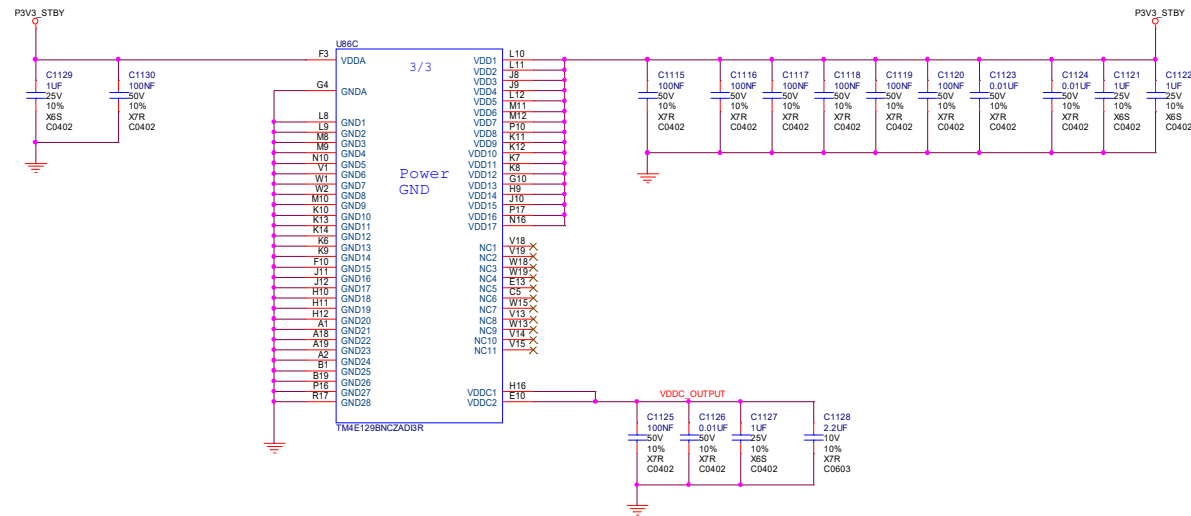


BIC_SNOWFLAKE 1

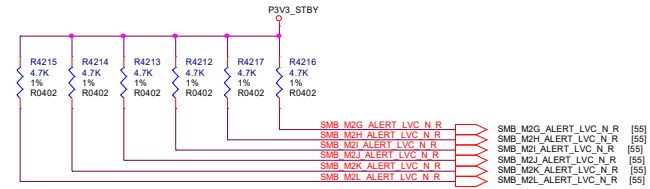
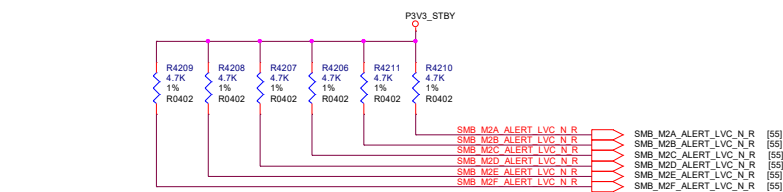
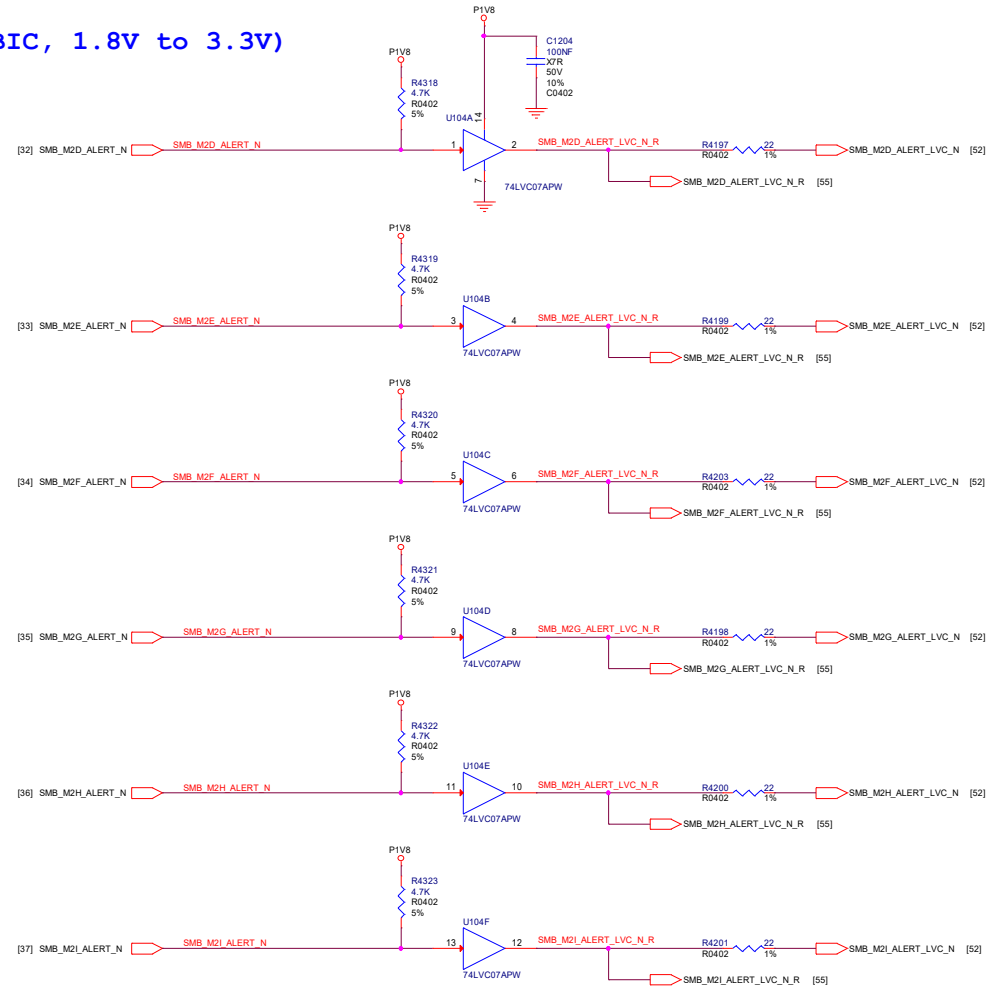


BIC Board ID						
Net Name	EVT	EVT2	EVT3	DVT1	DVT2	PVT
BIC_BOARD_ID_0	internal PU	1	0	1	0	1
BIC_BOARD_ID_1	internal PU	0	1	1	0	0
BIC_BOARD_ID_2	internal PU	0	0	0	1	1
0,1: HW PU PD						



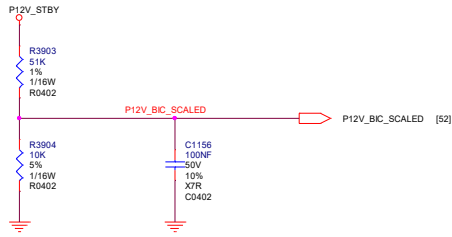


Level Shifter (M.2 to BIC, 1.8V to 3.3V)

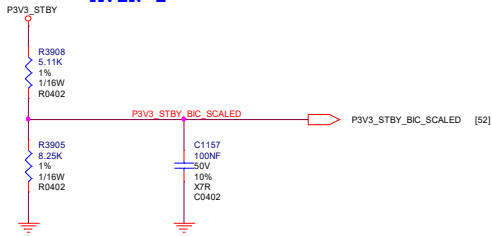


Level Shifter 4

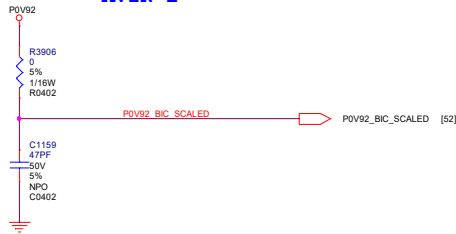
AVIN 0



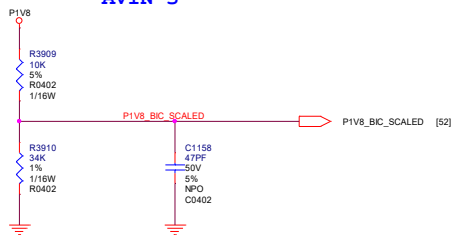
AVIN 1



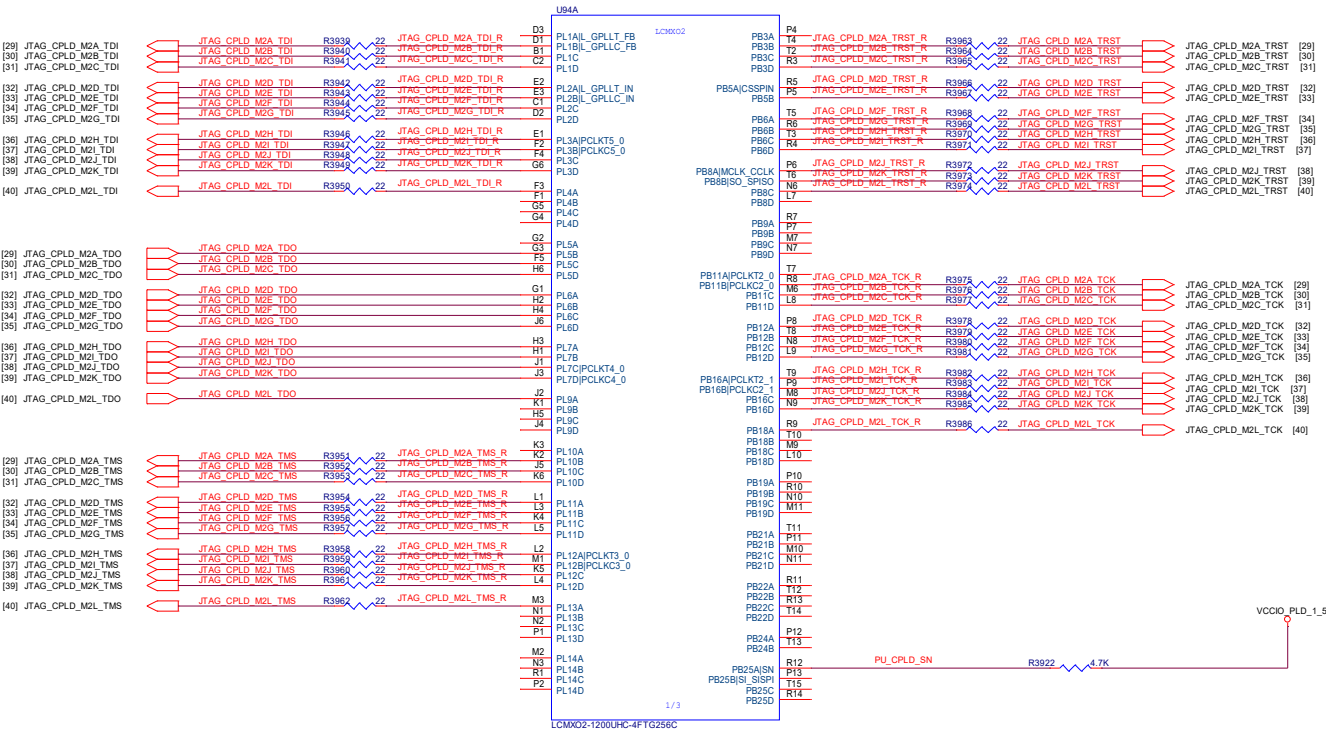
AVIN 2

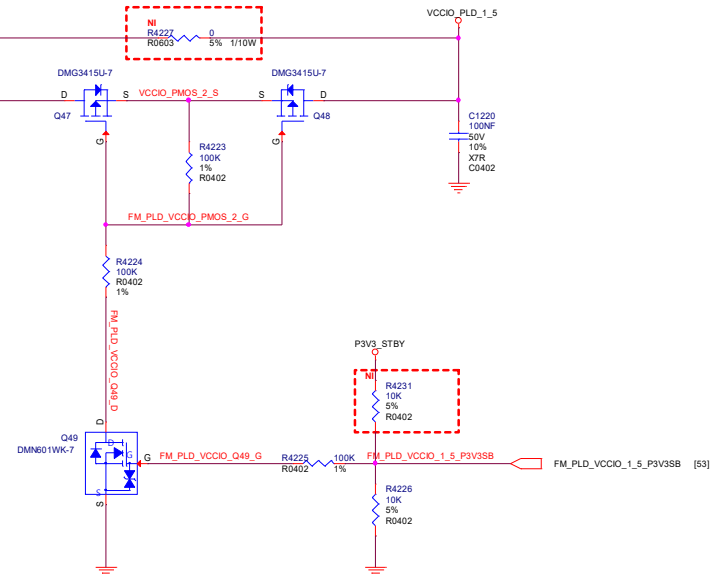
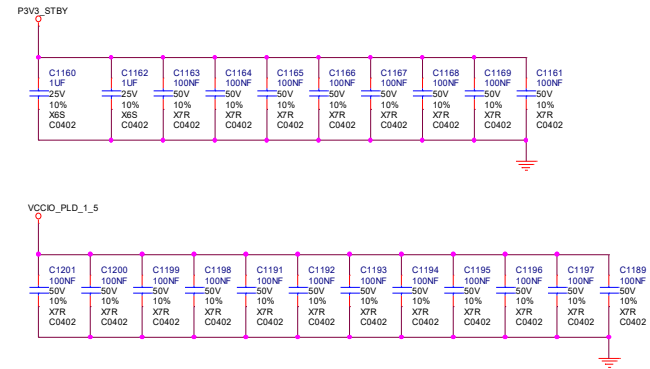


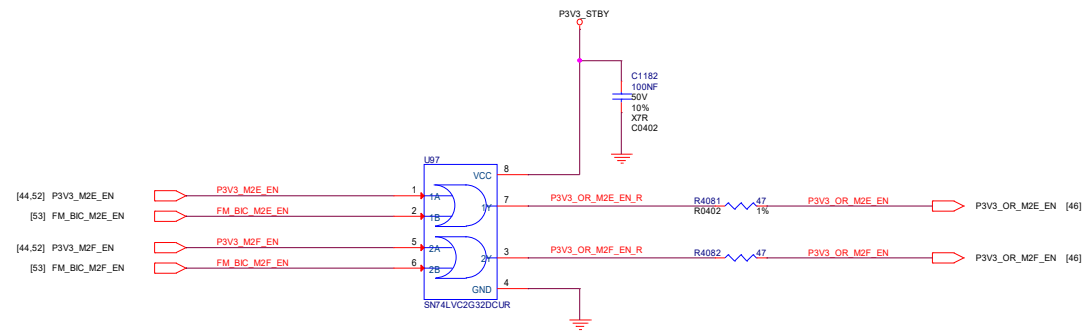
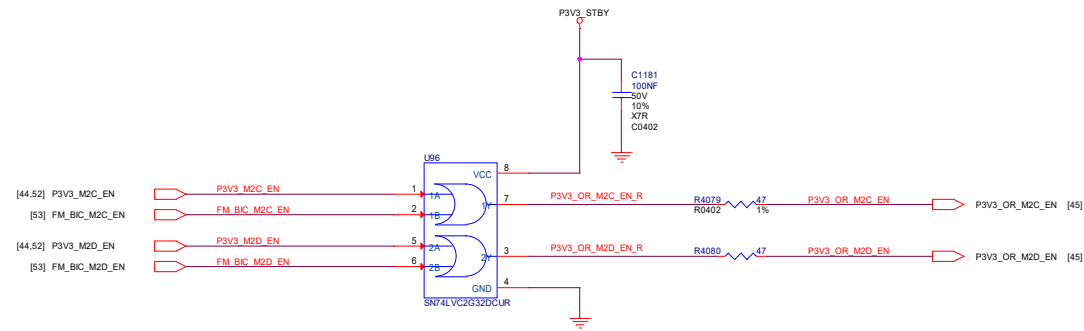
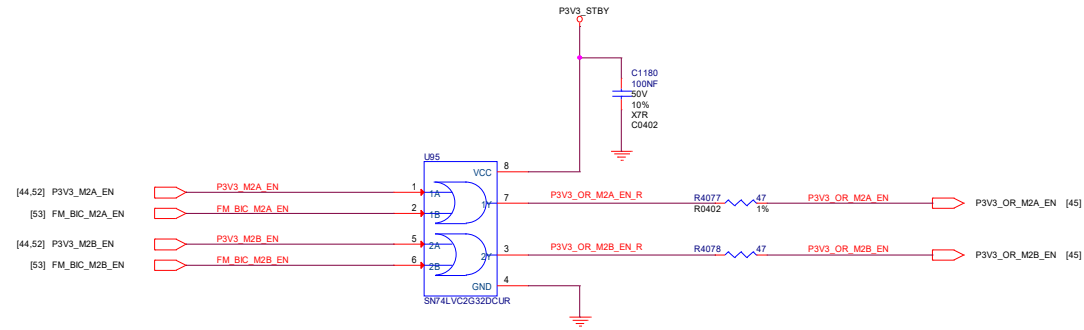
AVIN 3

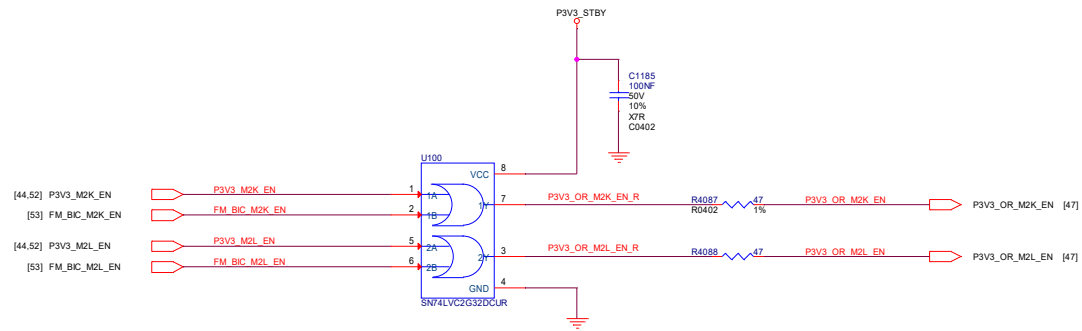
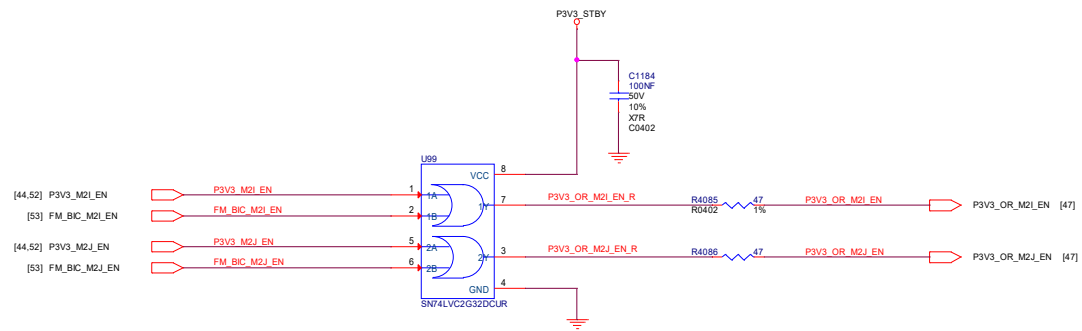
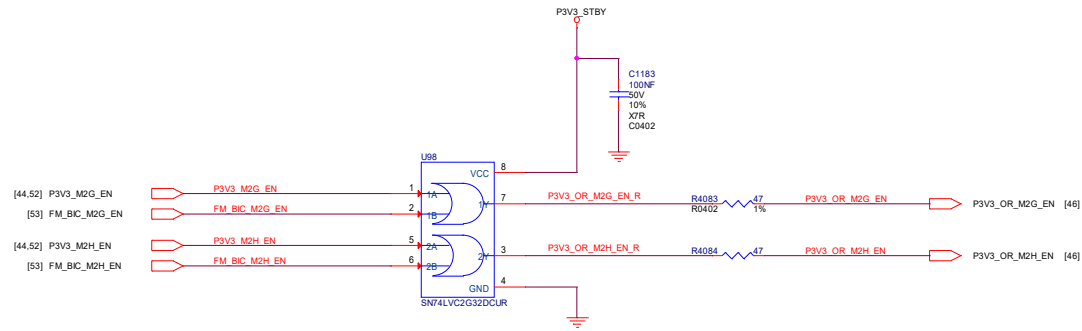


BIC-VOLTAGE MONITOR



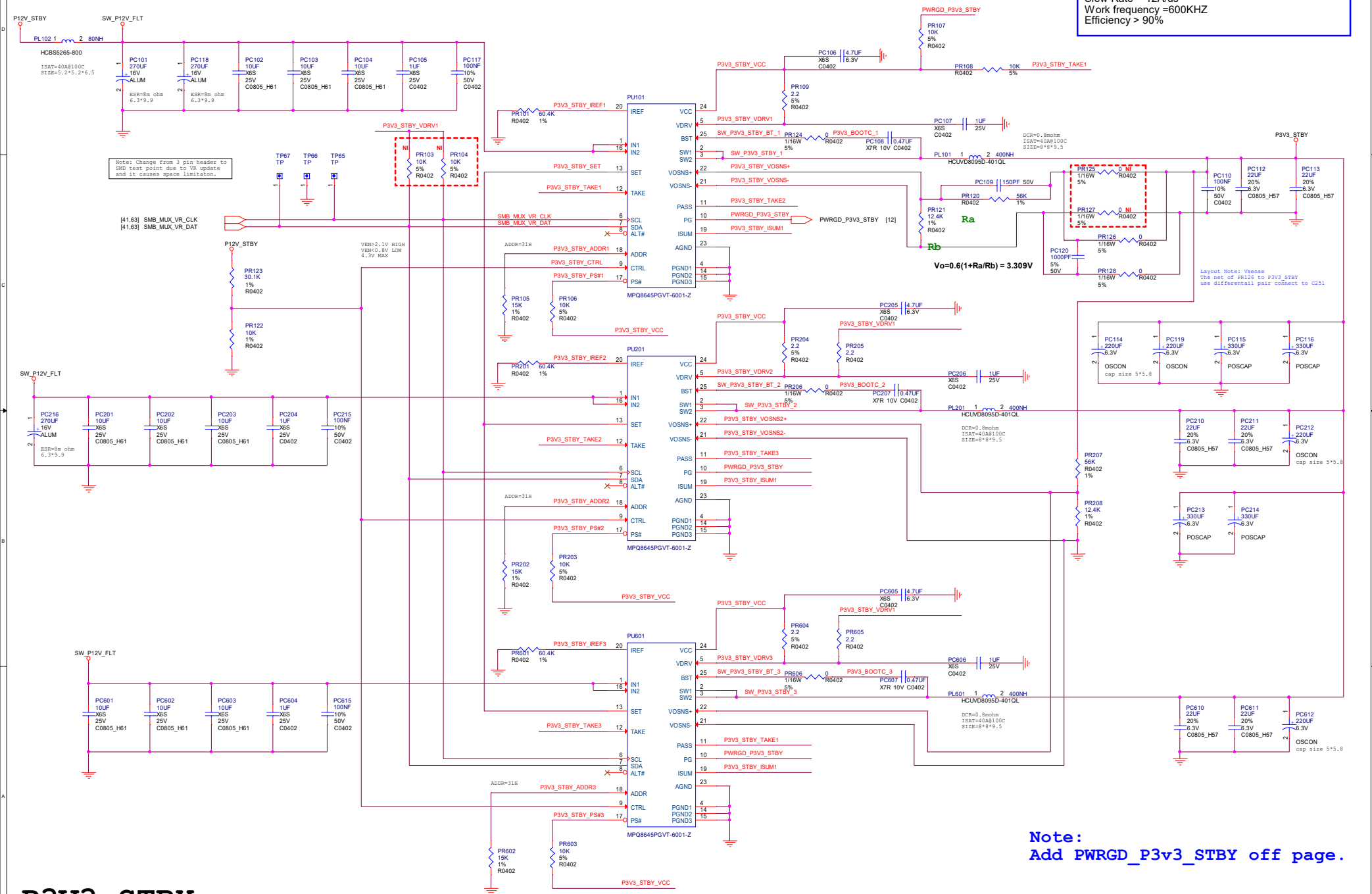






Design specification

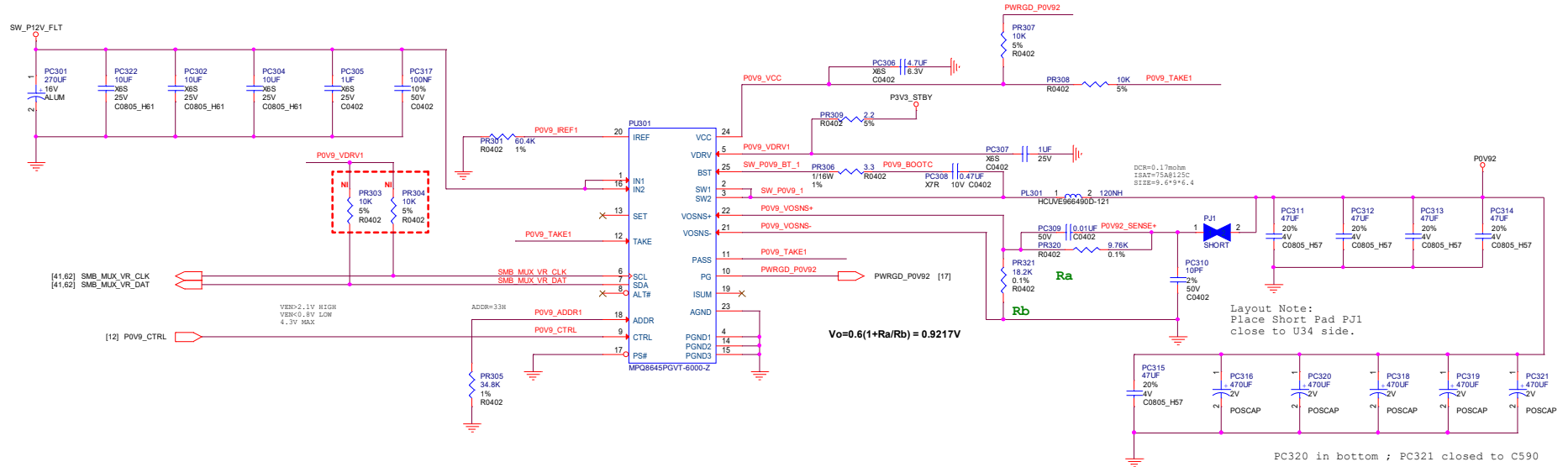
Output Voltage = 3.3 V +/- 5%
Output Ripple & Noise < 100mVpp
Transient Tolerance = 330mV
Max current = 43A ; (43A-73A for 20uS)
Over-Current Protection(Max Rating x1.2) = 87.6A
Current Step = 43-73A for 20uS, period time=1mS
Slew Rate = 12A/us
Work frequency = 600KHZ
Efficiency > 90%



P3V3 STBY

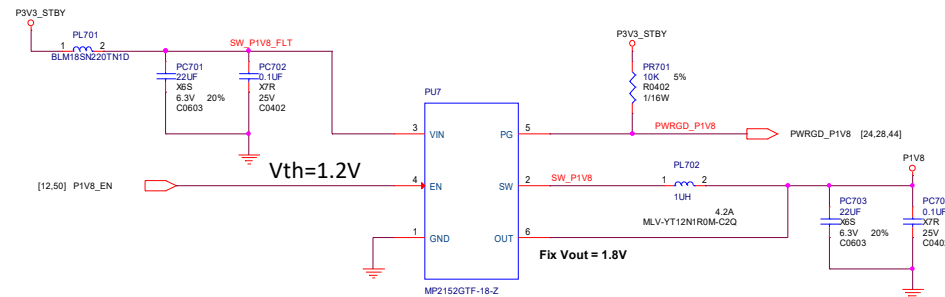
Design specification

Output Voltage = 0.92V $\pm$ 2.5%
 Output Ripple & Noise: <46mVpp
 Transient Tolerance = 46mV
 Max current = 30.27A
 Over-Current Protection(Max Rating x 1.3) = 40A
 Current Step = 15.5A (50% ~ 100%)
 Slew Rate = 2.5A/US
 Work frequency = 400KHZ
 Efficiency>80%
 Update date: 2018/11/19



Note:
Add PWRGD_P0V92 off page.

Design specification
P1V8
Output Voltage = 1.8V±5%
Output Ripple & Noise <180mVpp
Transient Tolerance = 180mV
Max current = 1.68A
Over-Current Protection(IC Rating) = 4A
Current Step = 1.0A
Slew Rate = 2.5A/us
Work Frequency = 1100kHz
Efficiency > 85% @TDC

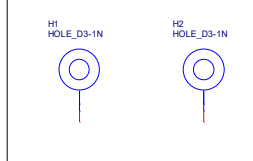


Note:
Add PWRGD_P1V8 off page.

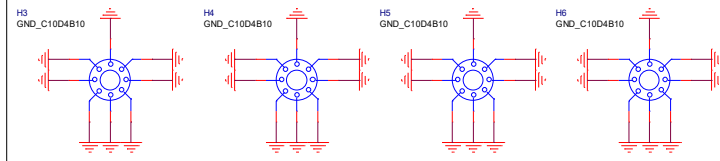
Note:
Add P1V8_EN offpage

Hole

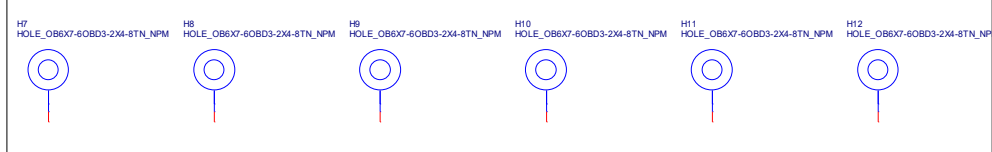
Heat Sink Hole X2



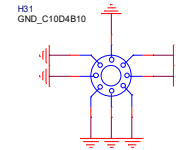
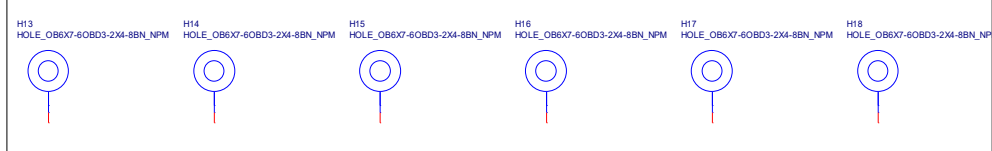
Ground Hole X4



Top Side X6

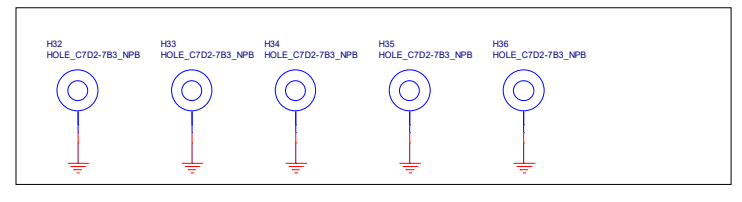


Bottom Side X6

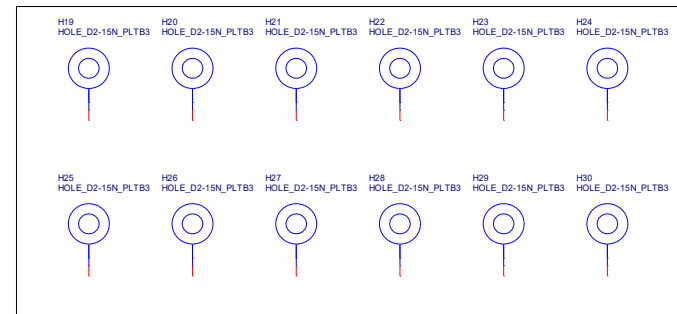


CAD Note:
#31 change to ground hole.

SMT NUT Hole: D2-7X5



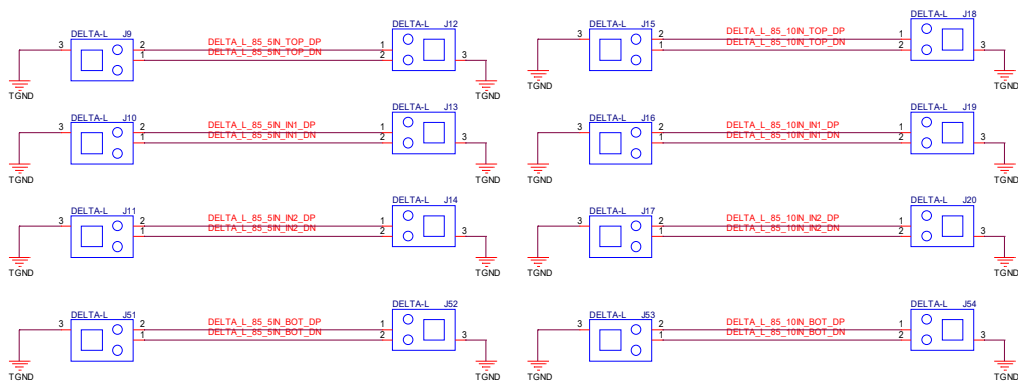
X12



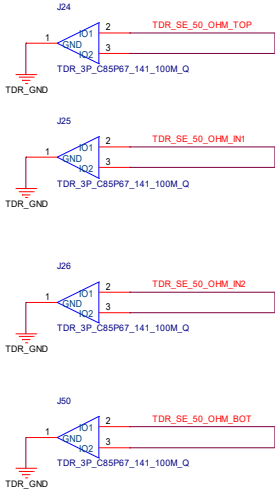
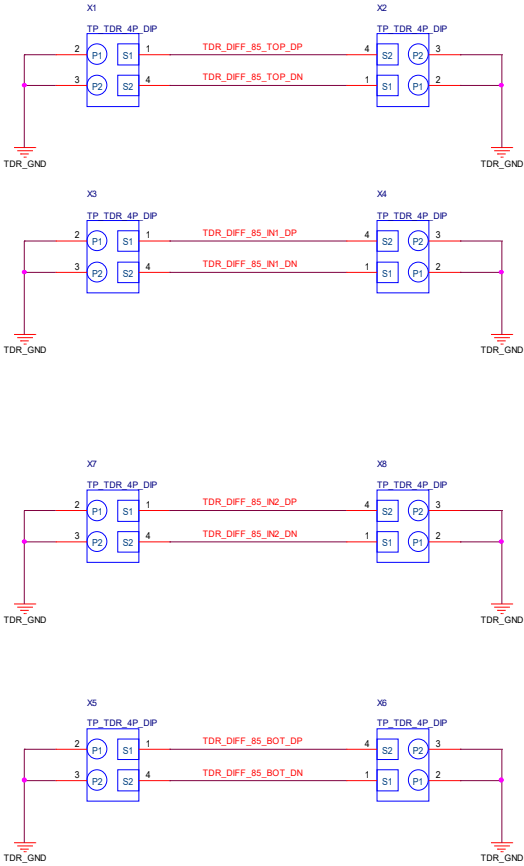
DELTA-L

5 INCH

10 INCH



TDR



DUMMY SYMBOL
PCIE SWITCH SPI FLASH

DM10
DUMMY_SYMBOL
PCIE_SWITCH_FLASH